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UNIVERSITÉ DE MONTRÉAL

DYNAMIC PUPIL REACTING TO INCIDENT LIGHT DEDICATED TO OCULAR IMPLANTS

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MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION
DU DIPLÔME DE MAÎTRISE ÈS SCIENCES APPLIQUÉES
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Ce mémoire intitulé:

DYNAMIC PUPIL REACTING TO INCIDENT LIGHT DEDICATED TO OCULAR IMPLANTS

présenté par: WEHBE Mohamad

en vue de l'obtention du diplôme de: Maîtrise ès sciences appliquées

a été dûment accepté par le jury d'examen constitué de:

M. LESAGE Frédéric, Ph.D., président

M. SAWAN Mohamad, Ph.D., membre et directeur de recherche

M. KASHYAP Raman, Ph.D., membre

"Human subtlety will never devise an invention more beautiful, more simple or more direct than does nature because in her inventions nothing is lacking, and nothing is superfluous."

Leonardo da Vinci

1452 - 1519

To my loving parents,

Raëf and Ghada

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Finally I would like to thank the Canadian Microelectronic Corporation for fabricating the chip and the NSERC for the financial support.

RÉSUMÉ

Une des fonctions de contrôle autonome de l'œil est d'adapter la luminosité aux différentes conditions extérieures pour une meilleure acuité visuelle. Ceci est fait en changeant la taille de la pupille.

La perte d'un œil est traumatisante peu importe l'âge. Elle a un grand impact sur l'image et l'estime de soi, ainsi que sur la confiance en soi. Bien que des solutions d'œil artificiel existent, elles ne sont qu'une amélioration esthétique et psychologique pour le patient, mais ne restaurent en aucune façon la vision. De plus un défaut d'anisocorie post-prothèse, c.à.d., la taille de la pupille qui ne change pas peu importe l'éclairage, apparaît avec un œil artificiel, ce qui produit un effet néfaste sur le patient.

Dans ce projet de maîtrise nous proposons de réduire le défaut d'anisocorie post-prothèse. Pour ce faire nous avons développé une pupille dynamique dédiée aux yeux artificiels. La pupille artificielle va en premier lieu capter la lumière ambiante à travers une photodiode, puis convertir le signal capté en un signal numérique pour déduire l'intensité lumineuse et finalement contrôler l'afficheur en conséquence. Ce système remplacera ainsi la pupille statique des yeux artificiels. Les résultats des simulations post-layout et expérimentaux nous ont permis de valider le bon fonctionnement du système. La partie principale du système a été implementée en utilisant la technologie CMOS 0.18 μm avec une superficie totale de 1.3 mm^2.

Un convertisseur analogique/numérique a été intégré au système, le rendant plus compact. En réalisant un convertisseur tension/courant, nous étions capable d'intégrer à notre système un convertisseur analogique/numérique ayant une entrée courant

développé par une équipe du laboratoire de neurotechnologies Polystim.

ABSTRACT

One of the autonomous control functions of the eye is to regulate light input to suit the conditions for best visual acuity. This is done by changing the size of the pupil. Losing an eye is devastating at any age. It has great impact on one's self image, self confidence and self esteem causing physical as well as psychological distress. A person who has lost an eye will replace the latter with an ocular implant. Standard ocular implants will attempt to faithfully reproduce the physical features of a natural eye, however the prosthetic pupil is fixed all the time giving a poor cosmetic appearance.

In this master's thesis we propose an artificial human pupil, which is composed of a dedicated controller and a miniaturized display. The purpose of this system is to overcome the problem of post-prosthesis anisocoria for people with ocular implants, by creating iris diaphragm in the prosthetic eye with photosensitive receptors responding to light so as to work in symmetry with the normal eye. The proposed artificial pupil would acquire ambient light through a photosensor, convert the acquired signal to digital data, transform this data to light intensity and finally control the display accordingly. This system would replace the static iris of a prosthetic eye. Experimental results from developed prototype, and post-layout simulation results from the integrated controller faithfully reproduce the expected performance, which is in the form of a dilating and contracting pupil. The main part of the system is implemented in 0.18 μm CMOS process and has a total area of 1.3 mm^2.

An analog-to-digital converter (ADC) has been integrated to the system, making it more compact. By developing a voltage-to-current converter we were able to use a current input ADC developed by a team of the Polystim neurotechnologies laboratory.

CONDENSÉ EN FRANÇAIS

Introduction

La majorité des déformations oculaires résultent de traumas, bien que dans 28.5% des cas, les tumeurs exigent l'énucléation de l'œil (Cheng *et al.* (2008)). Dans ces situations, les gens sont laissés avec un seul œil. Suite à la perte d'un œil, un implant est placé dans le globe oculaire pour faciliter la construction de la prothèse oculaire. Ceci est fait pour empêcher l'affaissement de l'orbite après l'énucléation.

Les implants oculaires ont subi des améliorations durant plusieurs décennies afin de fournir un remplacement esthétique pour l'œil énuclée (Beumer *et al.* (1979)). Malheureusement, les résultats esthétiques optimaux sont compromis quand la taille de la pupille choisie a un diamètre fixe peu importe les conditions d'éclairage.

Le diamètre de la pupille est très sensible à l'intensité lumineuse, et peut ainsi varier entre 2 mm et 8 mm. Ce phénomène est appelé l'anisocorie post-prothèse.

Des études ont été faites pour décrire la relation entre la taille de la pupille humaine et la densité de la lumière présente à la rétine (Spring and Stiles (1948), Groot and Gebhard (1952), Bergamin *et al.* (1998)). Groot and Gebhard (1952) ont dérivé une équation qui décrit cette relation :

$$\log d = 0.8558 - 0.0004(\log B + 8.1000)^3, \tag{1}$$

où d est le diamètre de la pupille en mm, et B est la luminosité en milliLamberts.

Dans ce projet de maîtrise, nous proposons de réduire le défaut d'anisocorie post-prothèse. Pour ce faire, nous avons développé une pupille dynamique dédiée aux yeux artificiels.

La pupille dynamique

Le prototype

Un prototype a été développé en vue de valider notre design avant la conception du système intégré. Ce prototype a été conçu avec des composantes électroniques discrètes.

Ce design peut être divisé en deux parties, soit une partie analogique et une partie numérique. La partie analogique est dédiée à la détection de la lumière. Elle comprend une photorésistance qui joue le rôle du capteur et une résistance variable pour ajuster la tension de sortie de cette partie.

La partie numérique est un contrôleur qui est basé sur un microcontrôleur (PIC 16F676) représentant un convertisseur analogique à numérique et effectuant trois fonctions essentielles, soit de convertir le signal analogique provenant du capteur en un signal numérique de 8 bits représentant la luminosité, puis de comparer cette valeur numérique à des valeurs mises en mémoire et finalement, de contrôler l'afficheur-simulant la pupille humaine.

La version intégrée

Ce système est constitué d'une photodiode, d'un contrôleur et d'un afficheur. Il peut être divisé en deux parties : la partie électronique de traitement de signal et la partie affichage reflétant le niveau de lumière reçu.

Partie électronique

Cette partie comprend un générateur d'horloge sur puce, un circuit de délai pour initialiser le système au démarrage, une unité de contrôle et finalement un convertisseur analogique/numérique.

- Générateur d'horloge

  Nous avons choisi l'architecture d'oscillateur en anneau à 7 étages pour générer le signal d'horloge requis. La fréquence d'oscillation est donnée par l'équation suivante :

  $$f_{osc} = \frac{1}{2N_{osc}\tau_{inv}} \tag{2}$$

  où N_{osc} est le nombre d'étages et τ_{inv} est le délai d'inversion pour chaque étage.

  Avec un délai d'inversion de $\tau_{inv} = 79.3$ ps, on obtient une fréquence d'oscillation de $f_{osc} = 900.9 \times MHz$.

  Un diviseur de fréquence comprenant des bascules D en série est utilisé pour ramener la fréquence à 100 kHz, la fréquence d'opération du convertisseur analogique/numérique.

- Le circuit d'initialisation

Ce circuit est utilisé pour initialiser le contrôleur au démarrage. Pour ce faire, ce circuit force un '0' logique sur le "reset" du contrôleur pour une certaine durée, pendant laquelle le système est remis à zéro.

Le circuit d'initialisation utilisé est un circuit de délai, illustré dans la figure 1.

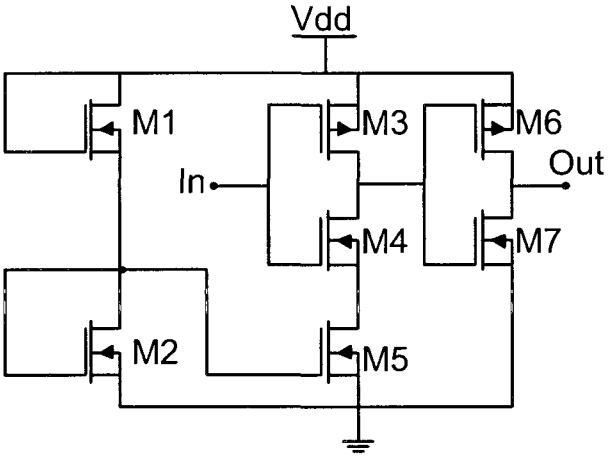

FIGURE 1: Le circuit de délai

L'unité principale de ce circuit est le tampon "current-starved" formé par les transistors M3 à M7. Le courant de chargement et de déchargement de la capacité de sortie est contrôlé par le miroir de courant constitué des transistors M2 et M5. Dès que le transistor M4 devient en état passant, sa capacité de sortie commence à décharger. Le courant de déchargement est contrôlé par M5 qui agit comme source de courant. Le courant passant dans ce dernier est contrôlé à son tour par la tension à la grille de M2. Cette tension est déterminée par le courant passant à travers le drain de M2. Le transistor M1 contrôle le courant passant par M2. Le ratio W/L de M1 a donc été conçu pour obtenir le délai voulu.

- Convertisseur analogique/numérique

Après avoir exploré les différentes architectures de CAN disponibles, nous avons jugé que le CAN à approximation successive est le meilleur choix pour notre système.

Ce CAN 8-bit de "Analog Devices" (figure 2) mesure de longueur 2.9 mm, de largeur 1.9 mm et une épaisseur de 0.9 mm, et peut donc être facilement intégré au prototype dy système.

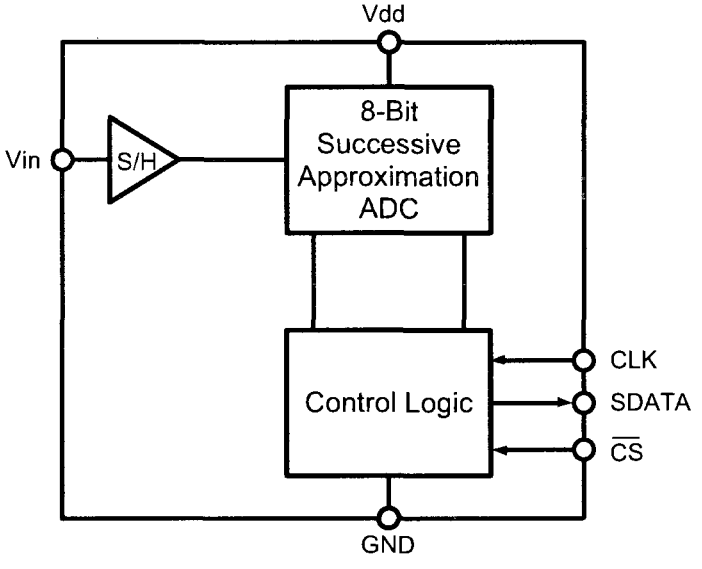

FIGURE 2: Diagramme bloc du CAN utilisé dans le premier prototype du système

Ce CAN est connecté directement à la photodiode, convertissant la sortie analogique de cette dernière en un signal numérique compatible avec le circuit numérique de contrôle.

L'acquisition des données et la conversion sont contrôlées par le signal $\overline{CS}$ et par l'horloge. Le signal d'entrée est échantillonné sur le front descendant de $\overline{CS}$, et la conversion est également initiée au même moment. La tension de référence est prise directement de V_{DD}, permettant une plage d'entrée plus grande. Par conséquent, la plage d'entrée analogique est de 0 V à V_{DD}.

- Le contrôleur

Le contrôleur est le module principal du présent système électronique. Celui-ci contrôle la contraction et la dilatation de la pupille prothétique. L'entrée de ce module provient de la sortie à 8 bits du CAN. Puisque la sortie du CAN est sérielle, un registre "serial-in/parallel-out" a été conçu pour connecter le contrôleur au CAN. Par la suite, le contrôleur transforme le signal numérique en intensité lumineuse, en se basant sur les données présentées au tableau 1.1. Ce module fournit trois niveaux d'animation pour la pupille prothétique, allant de complètement contractée à complètement dilatée. Pour atteindre une telle résolution, le contrôleur génère deux sorties codées en binaire.

Le contrôleur a été implémenté et testé en VHDL. L'algorithme implémenté compare l'entrée à des valeurs équivalentes à la luminosité dans le tableau 1.1, et, par la suite contrôle l'afficheur (pupille prothétique) en conséquence. L'algorithme a été synthétisé avec Design Vision (Synopsys, Inc.) pour générer un "netlist" du circuit. Le circuit physique a été créé par l'outil de placement-et-routage Soc-Encounter (Cadence).

L'algorithme utilisé dans le design du contrôleur est :

```
if (IN > 316 lux) then
     OUT1 = 0
     OUT2 = 0
     elsif (1 lux < IN < 316 lux) then
          OUT1 = 1
          OUT2 = 0
          else
            OUT1 = 1
```

```
                OUT2 = 1
endif;
```

L'afficheur

Avec la technologie d'aujourd'hui, le développement d'un afficheur à cristaux liquides ayant la taille de l'iris humain serait très dispendieux. Un compromis a donc été fait et l'afficheur simulant la pupille humaine a été développé en utilisant des diodes électroluminescentes (DEL). Les DELs utilisées ont une taille de 1.0 mm $\times$ 0.5 mm. Elles sont assemblées d'une manière circulaire, formant un afficheur ayant un diamètre de 12 mm, taille de l'iris humain. Une surface fixe de 4 mm^2 n'est pas influencée par la quantité de lumière; le capteur de lumière est installé dans cette région. La surface variable selon la lumière est un anneau ayant un diamètre intérieur de 2 mm et un diamètre total de 12 mm. Ainsi, selon la quantité de lumière, le diamètre de la pupille varie entre 2 mm et 12 mm.

La photodiode utilisée est une photodiode commerciale (TDK, Garden City, NY) ayant une taille de 1.5 mm $\times$ 2 mm, une sensibilité spectrale entre 350 et 750 nm et une plage de luminosité entre 0 et 75,000 Lux.

Les DELs forment deux cercles indépendants, fournissant trois niveaux d'animation. Ces deux cercles sont contrôlés par les deux sorties du contrôleur.

Résultats

Validation expérimentale du prototype

Le prototype a été assemblé sur un PCB utilisant des composantes discrètes, soit un microcontrôleur, une photorésistance, des transistors et des DELs. Le circuit schématique du circuit est illustré dans la figure 3.1 (chapitre 3). Le prototype a été testé dans différentes conditions d'éclairage, soit de l'éclairage faible à l'éclairage fort. Les résultats du test sont illustrés dans la figure 3.

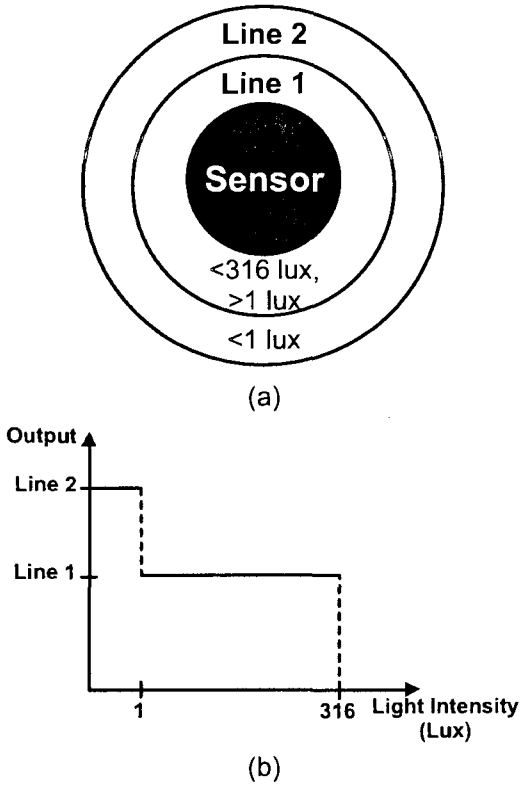

FIGURE 3: Résultats du test du prototype : (a) Diagramme d'intensité (b) Graphique illustrant la sortie du prototype

Lorsque la lumière est vive, les deux lignes sont désactivées. Lorsque l'éclairage est normal, seule la ligne 1 est active, tandis que les deux lignes sont actives lorsque l'éclairage est faible.

Dessins de masques

Une fois la conception schématique terminée, arrive l'étape du dessin de masques. En faisant le dessin de masques, on prend en considération l'apparition des résistances et des capacités parasites, les mésappariements et la capture du bruit provenant du substrat.

Résultats des simulations post-layout

Le circuit intégré a été conçu et fabriqué en utilisant la technologie CMOS 0.18 μm à puits n de la Taiwan (TSMC), ayant une superficie totale de 1.25 mm $\times$ 1.05 mm.

La première étape, lors de la vérification d'un circuit, est de valider son fonctionnement module par module, puis de vérifier la chaîne complète.

Le générateur d'horloge

La taille de ce module est de 95 μm $\times$ 57 μm. Ce dessin de masques comprend le "layout" de l'oscillateur en anneau avec le diviseur de fréquence. Tous les blocs sont entourés par deux anneaux de garde connectés respectivement à V_{DD} et V_{SS}. Les simulations post-layout de ce module ont donné un signal carré ayant une fréquence de 180 kHz.

Le circuit de délai

Ce module a été utilisé pour initialiser le système au démarrage, en appliquant un '0' au "reset" du contrôleur pour une période de 4 μs, après laquelle un '1' logique (1.8 V) est appliqué pour activer le circuit. À l'entrée de ce circuit, le signal V_{DD} est connecté.

Les résultats des simulations montrent le bon fonctionnement de ce circuit (figure 4).

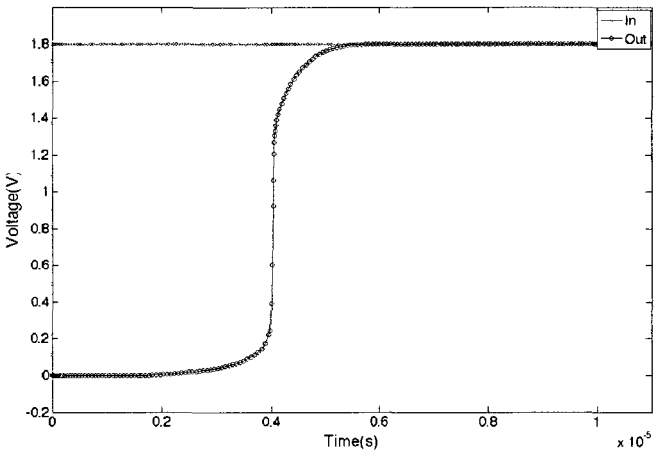

FIGURE 4: Résultats des simulations post-layout du circuit de délai

Le circuit de contrôle

Ce module est un contrôleur entièrement numérique, utilisant les blocs numériques fournis par la librairie "artisan" de la TSMC.

Le signal numérique provenant du CAN est appliqué à l'entrée de ce circuit. Ce signal contient de l'information sur l'intensité lumineuse. La sortie de ce circuit consiste en un mot de 2 bits contrôlant l'afficheur, tout comme dans le prototype.

Le circuit intégré

Après avoir validé le fonctionnement de chaque module seul, nous avons connecté tous les modules ensemble et testé la chaîne complète. Après la connection des différents modules, nous avons ajouté des pads et des plots de la librairie "tpz973g".

Le système a été simulé avec une tension d'alimentation de 1.8 V. Les résultats correspondent à nos attentes. Par la suite, le circuit a été testé avec différentes charges capacitives et résistives à la sortie.

Résultats expérimentaux

Un banc d'essai a été réalisé pour récupérer le signal d'horloge et les deux sorties du contrôleur. Le banc d'essai consistait en la mise à l'essai du CAN à approximation successive, de notre puce mentionnée ci-dessus, d'un capteur de lumière (photodiode), d'une source d'alimentation et d'un oscilloscope.

Premièrement, nous avons mesuré le signal d'horloge. Nous avons visualisé un signal ayant une amplitude de 1.76 V et une fréquence de 172 kHz. La puce a été testée comme montré dans la figure 4.11, et les résultats étaient identiques à ceux des simulations post-layout. Nous avons commencé le test avec une luminosité réduite, c'est-à-dire, une tension d'entrée près de 0 V, et les deux signaux de sortie étaient actifs, indiquant une pupille complètement dilatée. Par la suite, nous avons poursuivi le test avec une lumière vive, et les deux sorties du contrôleur étaient désactivées.

Le tableau 1 compare nos simulations post-layout avec les résultats expérimentaux.

TABLE 1: Paramètres simulés vs. paramètres mesurés

Paramètre	Simulé	Mesuré	|Erreur %|
Tension d'alimentation	1.8 V	1.8 V	N/A
Tension d'horloge	1.8 V	1.76 V	2.2 %
F_{CLK}	180 kHz	172 kHz	4.4 %
Tension de sortie	1.8 V	1.76 V	2.2 %
F_{OUT}	20 kHz	21 kHz	5 %
Rapport cyclique (sortie) %	20 %	13.5 %	32.5 %

Intégration du CAN

Une lacune de ce système était que le CAN n'était pas intégré dans la même puce que le reste des modules et qu'il occupait ainsi un espace important et augmentait la consommation de la puissance. Pour combler cette lacune, nous avons entrepris

l'étape d'intégration d'un CAN basse consommation d'énergie.

Le CAN intégré

Le CAN que nous avons intégré à notre puce est un CAN neuromimétique de 8 bits, qui a été développé par Yakoub (Yakoub *et al.* (2009)), membre de notre équipe de technologie Polystim. L'opération de ce CAN est inspirée de l'opération du neurone humain.

La figure 5 illustre le diagramme bloc de ce CAN.

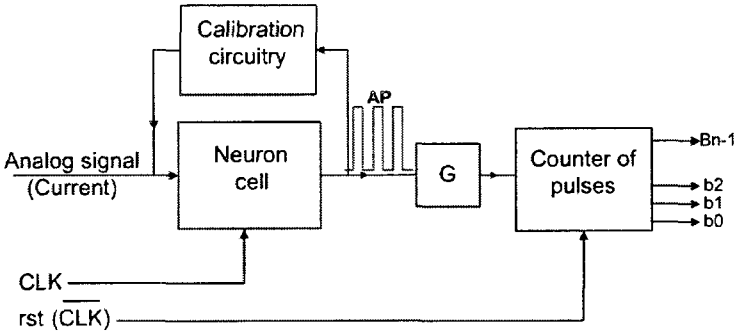

FIGURE 5: Diagramme bloc du CAN neuromimétique (Tiré de Yakoub *et al.* (2009))

Les blocs principaux qui constituent ce CAN sont la cellule neuronale, le circuit de calibration et le compteur.

L'entrée en courant de ce CAN est au niveau de la cellule neuronale. Cette dernière génère des impulsions en tension ayant une magnitude identique et une fréquence directement proportionnelle au courant d'entrée. Le circuit de calibration a pour fonction de satisfaire la proportionnalité entre le nombre d'impulsions et le courant d'entrée. Finalement, le compteur compte le nombre d'impulsions par une période de temps prédéfinie.

Convertisseur tension-courant

Étant donné que le CAN utilisé a une entrée en courant et que la photodiode a une sortie en tension, nous avons eu recours à un convertisseur tension-courant pour pouvoir faire la jonction entre ces deux modules. Le convertisseur tension-courant est un circuit "all-MOS" sans résistance (Fotouhi (2001)).

Ce convertisseur produit une sortie de courant qui est la somme des courants passant dans deux transistors opérant dans la zone linéaire et la zone de saturation. Un circuit schématique de ce convertisseur est montré dans la figure 5.4 (chapitre 5).

Résultats des simulations post-layout

Le convertisseur tension-courant et le CAN ont été conçus en utilisant la technologie CMOS 0.18 μm.

Nous avons simulé le convertisseur tension-courant avec une rampe allant de 0 V à 660 mV. Le courant de sortie de ce circuit (I_{out}) est directement proportionnel à cette rampe d'entrée (V_{in}). Cette relation est donnée par l'équation : $I_{out} = 2.65 \times 10^{-5}\ V_{in}$. Le convertisseur tension-courant atteint la saturation pour une entrée dépassant 660 mV, ce qui convient à notre application, la photodiode ayant une sortie entre 0 V et 650 mV.

Le courant de sortie de ce module varie entre 285 nA et 15.3 μA, également compatible à notre système, le CAN ayant une plage d'entrée entre 100 nA et 16 μA.

À la suite de la simulation du convertisseur tension-courant, nous avons couplé ce dernier avec le CAN. Nous avons connecté les 8 bits de sortie du CAN à un convertisseur numérique-analogique (CNA) idéal conçu en `veriloga`. Finalement, nous avons simulé la sortie du CNA qui représente une rampe reproduisant l'entrée.

À la suite de la simulation du convertisseur tension-courant et du CAN, nous avons testé le contrôleur couplé avec ces derniers. La figure 6 montre les résultats de simulation de l'ensemble du système. Ces résultats sont identiques aux résultats obtenus avec un CAN externe.

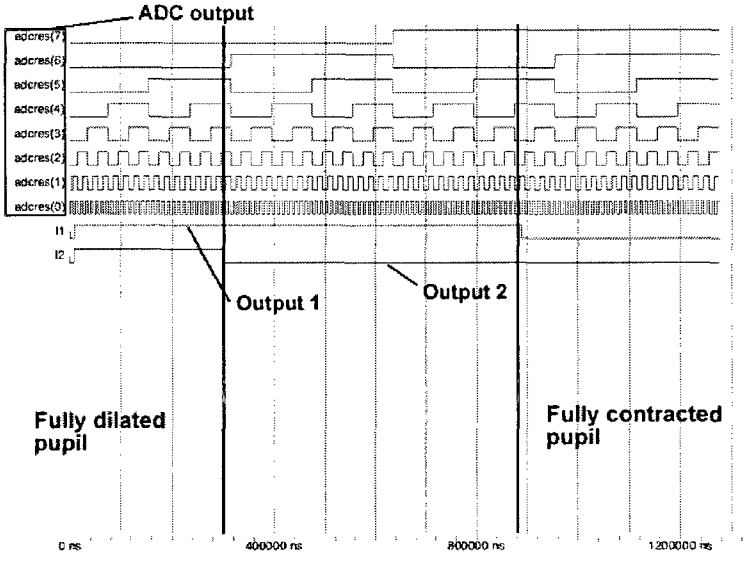

FIGURE 6: Résultats de simulation du système (contrôleur et du CAN)

Conclusion

Nous avons présenté, dans ce mémoire, un système d'implants oculaire pour les personnes ayant perdu un œil et qui désirent le remplacer par un œil artificiel qui ressemble à un œil normal. Ce système consiste en une pupille dynamique réagissant à la lumière incidente. Les résultats de simulation post-layout ainsi que les résultats expérimentaux ont montré le bon fonctionnement du système. Nous avons entre autres, proposé une version complètement intégrée du système qui regroupe un convertisseur analogique-numérique, mode courant et un convertisseur tension-courant pour diminuer la consommation de puissance et la taille occupée du système.

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LIST OF ABBREVIATIONS AND SYMBOLS

Abbreviations

ADC	Analog-to-Digital Converter
DAC	Digital-To-Analog Converter
DFF	D Fip-Fop
DNL	Differential Nonlinearity
DSP	Digital Signal Processing
EOG	Electro-oculograph
FPGA	Field-Prgrammable Gate Array
INL	Integral Nonlinearity
IR	Infra-Red
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
NC-ADC	Neuron Cell Analog-to-Digital Controller
OTA	Operational Transconductance Amplifier
PCB	Perforated Circuit Board
SAR	Successive Approximation Register
S/H	Sampling-and-Hold
UV	Ultra-Violet
VCC	Voltage-To-Current Converter

VST	Virtual Silicon Technology
WHO	World Health Organization

Symbols

h	$6.626069 \times 10^{-34} Js$ (Planck's constant)
ν	c/λ

LIST OF APPENDICES

INTRODUCTION

The majority of ocular defects result from traumas, although in 28.5% of the cases, tumors require the removal of the eye (Cheng *et al.* (2008)). So in these cases, people are left with one eye only. This is devastating at any age, having great impact on one's self image, self confidence and self esteem causing physical as well as psychological distress.

Frequently an implant is placed in the tissue bed to facilitate construction of the ocular prosthesis. This is done to prevent the eye socket from collapsing after enucleation. The art and science of ocular prosthetics has been refined over many decades to provide a cosmetic replacement for the enucleated or eviscerated eye (Beumer *et al.* (1979)). Unfortunately, cosmetic results are often compromised by the fixed pupil size. The pupil diameter is very sensitive to incident light intensity, and can vary from 2 mm to 8 mm in diameter depending on the light intensity. In ocular implants the fixed pupil is very noticeable. This is called post-prosthesis anisocoria.

Attempts have been made to simulate human pupil that adjusts to light level so as to dilate or contract with respect to ambient light. Several patents pertaining to developments in the field of ocular implants have been published (Young (2007), Budman and Stack (2003), Schleipman *et al.* (2000)).

The present master project deals with a dynamic prosthetic pupil to replace the static pupil that present-day ocular prosthesis have. This system would require a display that simulates the iris, a photodiode to measure the light quatity and a control system in order to be automated. In this master thesis a solution to overcome the problem of

post-prosthesis anisocoria is proposed; a prototype to validate the proposed solution is developed and tested. An integrated version is then designed, having an integrated circuit implemented and fabricated in the 0.18 μm CMOS technology.

Chapter 1 introduces some anatomical and physiological notion about the human eye and the pupil. We also introduce the ocular prosthesis, talk about the different types that exist, and the advances in the field.

Chapter 2 will be dealing with intelligent ocular implants, i.e., the kind of implants that render the eye prosthesis more realistic. Along this chapter we are going to describe work done in this field going from prosthetic eye movement to pupil size control.

Details of the development of the light controlled pupil are the subject of chapter 3. This chapter will discuss the different modules constituting the system. In this chapter a digital solution is proposed, the main purpose behind choosing such an approach is the ability to generate a square wave output with a controlled duty cycle in order to reduce the display activation time, therefore its energy consumption. This will be detailed in chapter 3.

Chapter 4 is devoted to the presentation of the results, from prototype results, analog layout techniques used, to the integrated circuit post-layout simulation results. The last chapter deals with improvements that we considered useful for the integration of the system and the reduction of power consumption.

CHAPTER 1

BACKGROUND

1.1 Introduction

In this chapter we give the necessary background information needed to understand the development of ocular implants and prosthetics, as well as some theory we were based on to develop the system.

This chapter is divided to three sections, namely: physiological background, ocular implants, and technical background.

1.2 Physiological Background

1.2.1 The Human Eye

The human eye is a complex anatomical organ. The eye is able to refract light and produce a focused image that can stimulate neural responses and enable the ability to see.

The eyeball is a slightly asymmetrical sphere, with an approximate sagittal diameter of 24 to 25 mm and a transverse diameter of 24 mm. A cross-sectional view of the eye shows three different layers, as illustrated in figure 1.1:

- The outer layer formed by the sclera and cornea
- The intermediate layer formed by the choroid

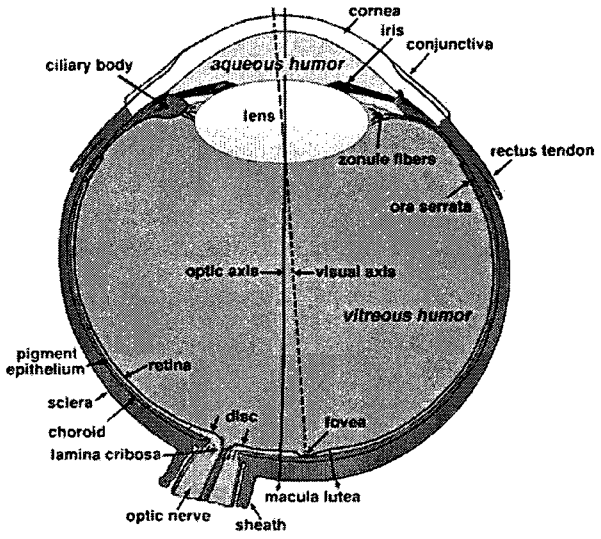


FIGURE 1.1: A cross-sectional view of the human eye

- The inner layer formed by the retina

Three chambers of fluid are also found in the eye:

- The anterior chamber found between the cornea and the iris
- The posterior chamber found between the iris, zonule fibers and the lens
- The vitreous chamber found between the lens and the retina

The first two chambers are filled with aqueous humor whereas the vitreous chamber is filled with a more viscous fluid, the vitreous humor.

After giving a brief description of the gross anatomy of the eye, now we are interested in a closer description of the pupil and its function.

1.2.1.1 The Pupil

The pupil is the sphere that is located in the center of the iris of the eye, as shown in figure 1.2. When functioning normally, the pupil is linked with a feedback-mechanism in the central nervous system, which controls the quantity of light crossing the lens and reaching the retina (Zinn (1972)). The size of the pupil influences also the depth of focus.

The iris controls the amount of light entering the eye. Irises are pigmented with melanin, and their dimensions vary slightly between individuals, but on average they are 12 mm in diameter. Due to its heavy pigmentation, light can only pass through the iris via the pupil (Lefohn *et al.* (2003)).

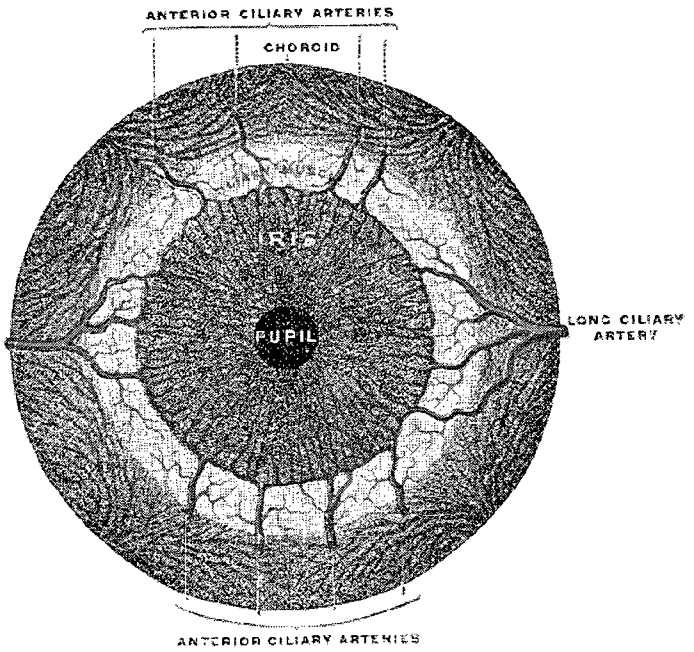


FIGURE 1.2: A frontal view of the human iris (adapted from: Gray (1918))

The aperture of the eye is controlled by the iris that behaves as a diaphragm, either contracting or dilating as a result of the opposing actions of two ectodermal muscles (Davson (1972)).

In general the pupil size varies approximately from 2 to 8 mm in diameter. A pupil of varying size performs three main functions:

- Modifying the amount of light entering the eye, thus permittimg useful vision over a wide range of luminance levels.
- Adapting the depth of focus for near and far objects.
- Minimizing abberations.

The factors that affect the size of the pupil are grouped into mechanical, extrinsic and intrinsic factors. Given that the mechanical and the intrinsic factors are purely physiological and congenital factors, hence of no interest to this work, we will only discuss the extrinsic factors.

Extrinsic factors cause what is known as pupillary light reflex. Pupillary light reflex is an innervation reflex that controls the size of the pupil in response to light intensity falling on the retina of the eye (Purves *et al.* (2008)). Greater light intensity causes the pupil to become smaller, allowing less light in, whereas lower light intensity causes the pupil to become larger, allowing more light in. In other words, the pupillary light reflex regulates the light quantity entering the eye.

1.2.2 Pathologies

A list containing every known eye disease and disorder is published by the World Health Organization (WHO) in the International Statistical Classification of Diseases and Related Health Problems (ICD-10), however we are only interested in a disorder called anisocoria.

Anisocoria is a condition characterized by an unequal size of pupils. Causes of anisocoria are varied, it could be pathophysiologic, pharmacologic, mechanical, self induced

etc. According to the Merck manual of diagnosis, about 20 % of people have physiologic anisocoria. Self induced anisocoria also known as post-prosthesis anisocoria is present in persons who have lost an eye, and replaced the latter with an ocular implant. The ocular implant has a fixed pupil size all the time, while the natural eye has a normal pupil, this causes a difference in the size of the pupils.

1.2.3 Pupil Size vs. Ambient Light

Studies have been made to describe the relationship between the size of the human pupil and the density of the incident light on the retina (Spring and Stiles (1948), Groot and Gebhard (1952), Bergamin *et al.* (1998)). De Groot and Gebhard have derived a relation between the diameter of the human pupil and the intensity of the incident light. This relation is illustrated by

$$\log d = 0.8558 - 0.0004(\log B + 8.1000)^3, \tag{1.1}$$

where d is the diameter of the pupil in millimeters and B is the luminance of the visual field in millilamberts. This relation was used in the development of our system. Table 1.1 summarizes the values we got from equation (1.1). In table 1.1 we converted the *millilamberts* to *lux*, since the lux is the SI unit of illuminance (NIST (2000)). For a better understanding of these values some explanations should be given. A 3,000 *lux* intensity is the luminance our eyes experience in the outdoor morning light (Figueiro *et al.* (2007)). Looking directly to bright sun our eyes experience a luminance of 100,000 *lux*. However an intensity like this could damage the human eye. Buildings interior and bright offices have a typical intensity between 100 and 500 *lux*, and a dim room has a light density of less than 1 *lux*.

TABLE 1.1: Pupil size with respect to light intensity

Luminance (*Lux*)	**Pupil diameter** (*mm*)	**Luminance** (*Lux*)	**Pupil diameter** (*mm*)
0.000010	7.12	10.00000	4.39
0.000100	6.98	31.62278	3.99
0.001000	6.73	100.0000	3.59
1.000000	5.15	316.2277	3.17
3.162278	4.78	19952.62	1.87

1.3 Ocular Prosthetics

An ocular prosthesis or artificial eye replaces an absent natural eye following an enucleation, or evisceration (Beumer *et al.* (1979)). Enucleation is the surgical removal of the eye ball, leaving the eye muscles and remaining orbital contents intact; while evisceration is the surgical evacuation of the entire contents of the eye ball including the cornea. An artificial eye does not provide sight, it fills the cavity of the eye socket and serves only as a cosmetic enhancement with psychological impact on the patient.

The objectives behind fitting a prosthesis after one has lost an eye could be as follows (Prince (1946)):

- To maintain the shape of the eyelid
- To re-establish full lid movement
- To prevent fluid accumulation in the cavity
- For Cosmetic purposes.

The last reason is the most important one as far as the patient is concerned, unless a detailed explanation about the other reasons is added.

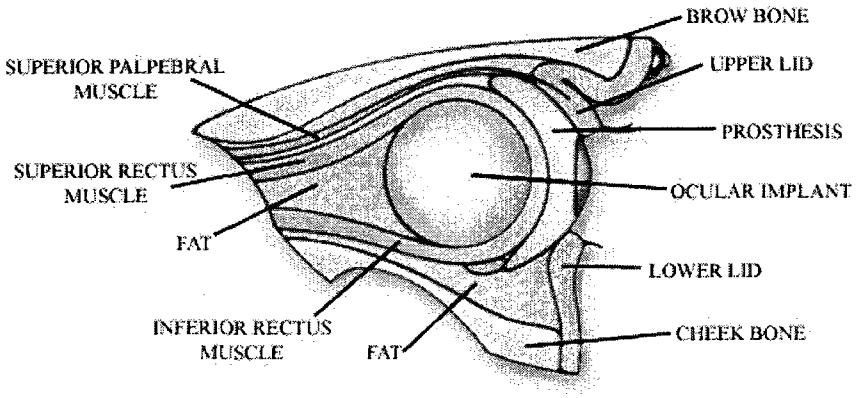


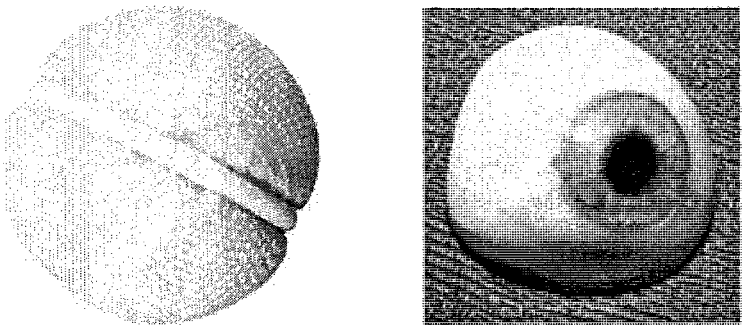
FIGURE 1.3: A drawing of the ocular implant with the prosthesis (adapted from Erickson's Artificial Eyes: http://www.ericksons-eyes.com)

In most cases an ocular implant, or orbital implant, is used to fill the area in the orbit that was occupied by the natural eye as shown in figure 1.3. This spherical implant will maintain the natural structure of the orbit and will provide support for the artificial eye. The ocular implant itself is not visible.

An ocular prosthesis, or artificial eye, is the element that is seen by the outside world, and it is used to restore the natural appearance of the eye and surrounding tissues. Ocular implants are usually made of acrylic or glass.

More natural appearances were achieved by the developpement of hydroxyapatite for ocular implants. Hydroxyapatite is a bioceramic having mineral components similar to bones of the human body, and has the ability to chemically interact with it (Hench (1991), Gittings *et al.* (2009)). Thus, once implanted, the tissues of the eye orbit will grow into the hydroxyapatite implants, which will become a part of the body.

Different types of implants have existed, and can be categorized based on the implant material (porous or nonporous, alloplastic or autogenous) and its relationship to the overlying prosthesis (integrated or non-integrated, buried or exposed) (Rubin *et al.* (1998)). In the following section we will discuss some of the main types of ocular implants.



(a) (b)

FIGURE 1.4: Full artificial eye prosthesis: (a) a bio-ceramic orbital implant, (b) the eye prosthesis

1.3.1 Types of Ocular Implants

1.3.1.1 Full Artificial Eye Prosthesis

When an eye is removed (after enucleation), surgeons typically place a small round implant (figure 1.4 (a)) into the orbit and connect it to the eye muscles around it to hold it in place (Adkinsson (2006)). This implant takes the place of the eye in the orbit. Against this implant, a prosthesis resembling the natural eye (figure 1.4 (b)) will fit.

The implants are usually made from acrylic, or glass. Other implants made from materials such as coral, hydroxyapatite or perforated plastic exist, with the idea that the muscles will grow into them allowing the implant to move, mimicking the natural eye. These implants typically have a titanium peg protruding forward from the implant upon which the prosthesis rests.

1.3.1.2 Scleral Shell

Many people lose the sight in one eye, without losing the eye itself. Following sight loss, the eye will start to shrink, discolor, or move erratically. In these situations a

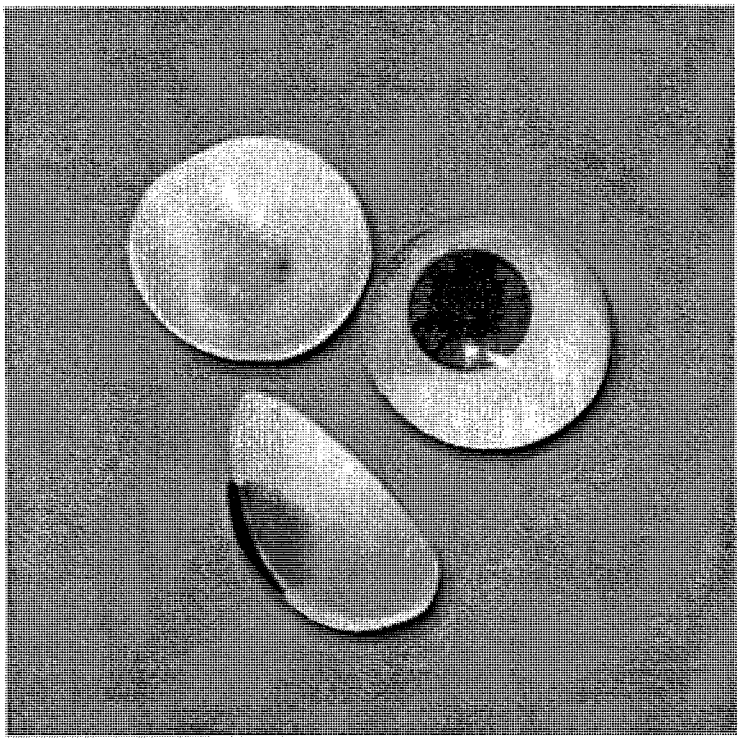


FIGURE 1.5: Scleral shell prosthesis

scleral shell is proposed.

The scleral shell (figure 1.5) is a custom-made, thin hard acrylic shell-like eye prosthesis fitted directly over a discolored and/or disfigured eye. It includes the iris and the sclera (Anonymous (2009)). This prosthesis will help restore volume loss, and will assist the upper lid to return to normal position, matching the natural eye. Good motility is obtained usually with scleral shells.

1.3.2 Advances in Ocular Prosthetics

Artificial eyes have seen little change over the years. Originally made from glass, ocularists started using synthetic materials in the 1940s. Although several improvements have been reported in the manufacturing of ocular prosthesis, the fabrication methods currently in use are based on obsolete technologies, lack high degree of precision and

are time-consuming (Shah and Aeran (2008)). Examples of advances in the field of ocular prosthesis include a magnetically coupled implant and prosthesis as described by Garonzik (2001). The orbital implant is inserted in the empty eye socket, and the eye prosthesis is coupled magnetically to the implant overcoming problems associated with the use of a coupling post such as the extrusion of the implant and conjunctival erosion. Furthermore, a self-lubricating ocular prosthesis has been designed that releases a lubricant continuously on the surface of the prosthesis, eliminating dry eye syndrome, burning and itching (Kelley (1992)). Recent development in the ocular prosthesis fabrication include the use of specially developed biomaterials to reduce any allergic reaction. Development in this field also includes realistic modelling and rendering in iris synthesis (Lefohn *et al.* (2003)).

1.4 Technical Background

1.4.1 Optical Detectors and Receivers

This section describes the operating principles of optical detectors. Optical detectors can be classified by their principle of light detection: physical or chemical changes, solid or gas ionization, scintillation, and photoelectric effect (Dakin and Brown (2006)). Detectors utilizing physical or chemical changes are photographic films, and are rarely used nowadays in photometric applications. Methods utilising solid or gas ionization and scintillation are usually limited to x-ray applications.

Photodetectors with photoelectric effects are widely used as Ultra-Violet (UV) to Infra-Red (IR) sensors in application including communication devices and measurement instruments.

Because of space restrictions, we will only disccuss the photodetectors utilising the photoelectric effects.

1.4.1.1 Photoelectric Effects

Optical detectors utilizing these effects can be further divided into two groups: one group using external photoelectric effects by which bound electrons inside a semiconductor thin film are released into vacuum when light hits the semiconductor, and the other one using internal photoelectric effects where photoelectrons are generated inside the semiconductor by light and excited into the conduction band (Sommer (1980), Bube (1992)).

1.4.1.1.1 External Photoelectric Effect

Optical detectors utilizing external photoelectric effects include phototubes, photomultiplier tubes and image intensifiers (Dakin and Brown (2006)).

Semiconductor thin films with a photoemissive surface are usually referred to as "photocathodes" (Sommer (1980)). A general band model of photocathodes is illustrated in figure 1.6. Inside a semiconductor there is what is known as a valence band which is occupied by electrons, a forbidden band where electrons connot occupy, and a conduction band where electron have the freedom to move.

When photons hit a photocathode, electrons in the valence band absorb the photon energy $h\nu$, become excited into the conduction band, and diffuse toward the surface. When a diffused electron has enough energy to overcome the vacuum level, it is emitted into the vacuum as photoelectron.

1.4.1.1.2 Internal Photoelectric Effect

Photodetectors using internal photoelectric effects include photodiodes, phototransistors, and photoconductive cells. Photoelectric effect include both photoconductive effect, and photovoltaic effect (Dakin and Brown (2006)). However, we will focus on

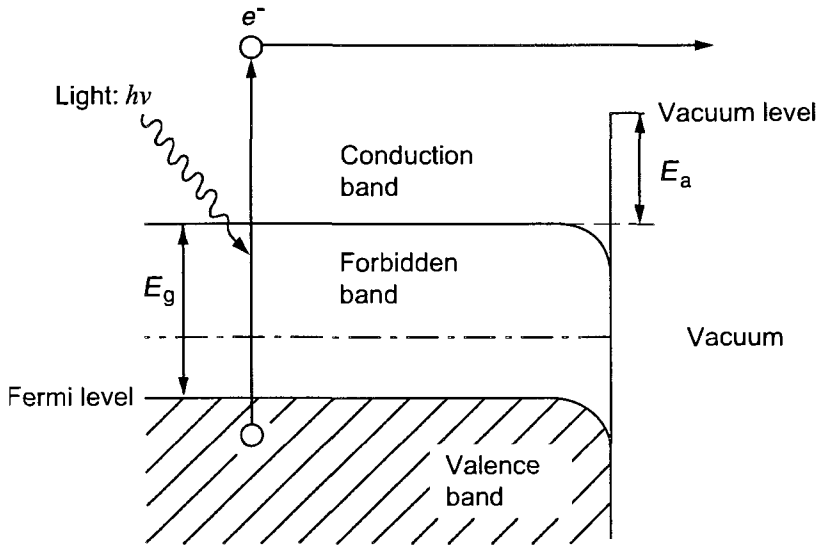


FIGURE 1.6: Photocathodes band model (Adapted from Dakin and Brown (2006)

the photovoltaic effect in this section.

The photovoltaic effect will be explained using a photodiode example. Figure 1.7 shows a cross-section of a photodiode.

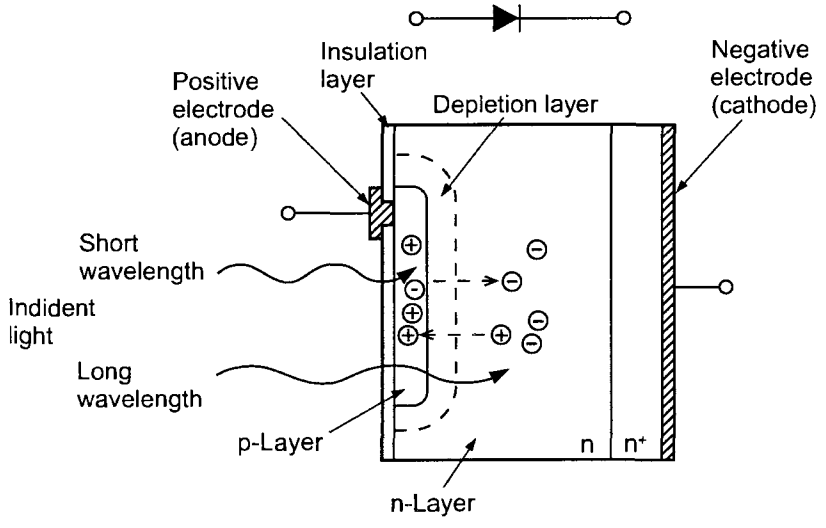


FIGURE 1.7: Photodiode cross-section (Adapted from Dakin and Brown (2006)

A *p-n* junction serving as a photoelectric converter is formed by the p-layer at the

light sensitive surface and the n-layer at the substrate. The photodiode's spectral and frequency responses can be controlled by varying the thickness of the outer p-layer, substrate n-layer and bottom N^+ layer as well as the doping concentration.

When light striking the photodiode has an energy greater than the band gap energy, electrons in the valence band are excited into the conduction band, leaving holes in their place in the valence band. The electron-hole pairs are generated in the p-layer, depletion layer and n-layer. The electric field in the p-layer and depletion layer accelerates the holes toward the p-layer, and the electrons toward the n-layer. In the n-layer, of the electron-hole pairs generated, the electrons are left in the n-layer along with electrons coming from the p-layer, and the holes are collected in the p-layer. This way, electron-hole pairs generated proportionaly to the amount of incident light are stored in the p-layer and n-layer, creating a positive charge in the p-layer and a negative charge in the n-layer. So by connecting a circuit between the p-layer and the n-layer, holes will flow from the p-layer and electrons from the n-layer toward the opposite electrode.

1.4.2 Main Types of Oscillators

The characteristics we are looking for in an oscillator for the proposed device are low output noise, low power consumption and integrability. Different types of oscillators exist in the literature, here we are going to describe the most appropriate for the proposed device.

1.4.2.1 LC Oscillator

In an LC circuit, the frequency f_{lc} at which the circuit resonates is given by the following equation(Mansour *et al.* (2004), Sadat *et al.* (2005)):

$$f_{lc} = \frac{1}{2\pi\sqrt{LC}} \tag{1.2}$$

The LC oscillator is shown in the circuit illustrated in figure 1.8.

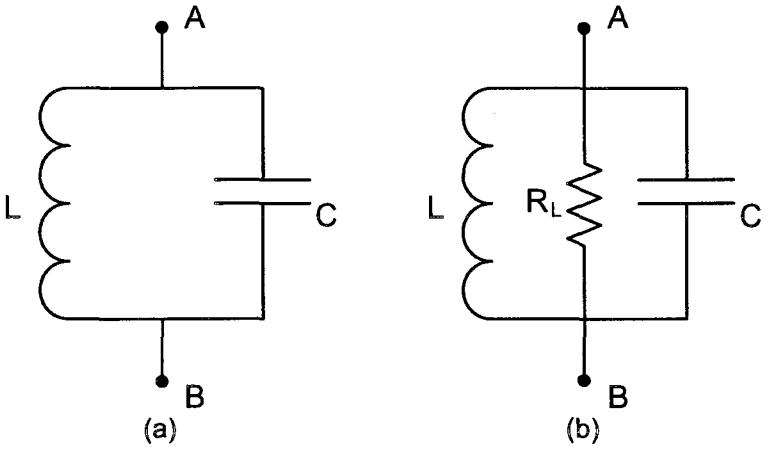


FIGURE 1.8: LC oscillator: (a) ideal model and (b) real model

In the real model, the inductance L has a small parasitic resistance R_L as shown in the figure 1.8 (b). Due to this resistance, some energy stored in the reactive element will be dissipated in R_L as heat, and as a result, the oscillation dies. Now if we connect a negative resistance to the LC tank, the energy lost in R_L will be compensated for by the energy supplied by the negative resistance, thus the circuit oscillates. This negative resistance is usually synthesized by a differential pair.

An LC oscillator could be divided into three different parts: the RLC circuit, a differential pair and a variable capacitor.

- **The RLC circuit** is the core of the oscillator since it defines the resonance frequency.
- **The differential pair** allows the system to oscillate by generating a negative resistance.

- **The variable capacitor** allows for the oscillator to have a certain excursion range in the frequency.

The advantage of using such oscillators is the signal quality. In fact their output signal has low phase noise compared to other types of oscillators. However, two main drawbacks may prevent, sometimes, from choosing this type of oscillators (Fouzar (2005)). These drawbacks are their limited excursion range and their cost.

1.4.2.2 Relaxation Oscillator

This type of oscillators contains usually two essential parts: a comparator with hysteresis (schmitt inverter) and a capacitor, as shown in figure 1.9. The principle of operation consists of charging and discharging a capacitor in a voltage interval defined by the threshold voltages of the comparator. At startup, the voltage across C is zero, and the output of the inverter is high. The capacitor then starts charging up via R. When the capacitor's voltage reaches the high voltage threshold of the inverter, V_H, the output of the inverter goes low. With the output low, C starts discharging toward 0V. When the capacitor's voltage drops below the low voltage threshold of the inverter, V_L, the output goes high. The cycle repeats. The half-period of the oscillations is defined by the time the capacitor's voltage takes to go from V_L to V_H. The other half depends on the time needed to go from V_H to V_L.

As a result, the frequency of oscillations (f_{osc}) is determined by the high-going and low-going threshold voltages and the RC time constant. This relation is defined by the following equation (Wokhlu *et al.* (1998)):

$$f_{osc} = \frac{1}{T_{osc}} = \frac{1}{RC\ln([\frac{V_H}{V_L}][\frac{V_{dd}-V_L}{V_{dd}-V_H}])} \tag{1.3}$$

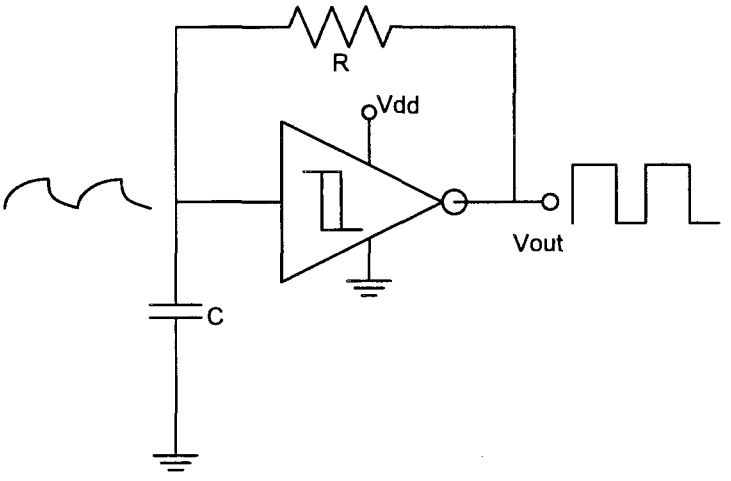


FIGURE 1.9: Relaxation oscillator based on Schmitt Trigger

where C is the capacitor, R is the resistor, and V_{t-l} and V_{t-h} are the minimal and maximal voltage thresholds, respectively.

Compared to LC oscillators, the relaxation oscillators offer a larger frequency excursion range, and could be easily integrated on a chip (Fouzar (2005)). However, they do suffer from output phase noise, which could limit their use in some applications.

1.4.2.3 Ring Oscillator

This type of oscillators is formed by a finite number of inverters, N_{osc}, in cascade, forming a reaction loop. The ring oscillator requires an odd number of inverters in its loop to generate oscillations. This type of oscillators uses the principle of charging and discharching its intrinsic capacitances to generate oscillations at its output. Figure 1.10 (a) illustrates this type of circuits.

In the loop forming this circuit, the phase of each inverter is shifted relatively to neighboring inverters. During each half period, $T_{osc}/2$, a signal is propagated through

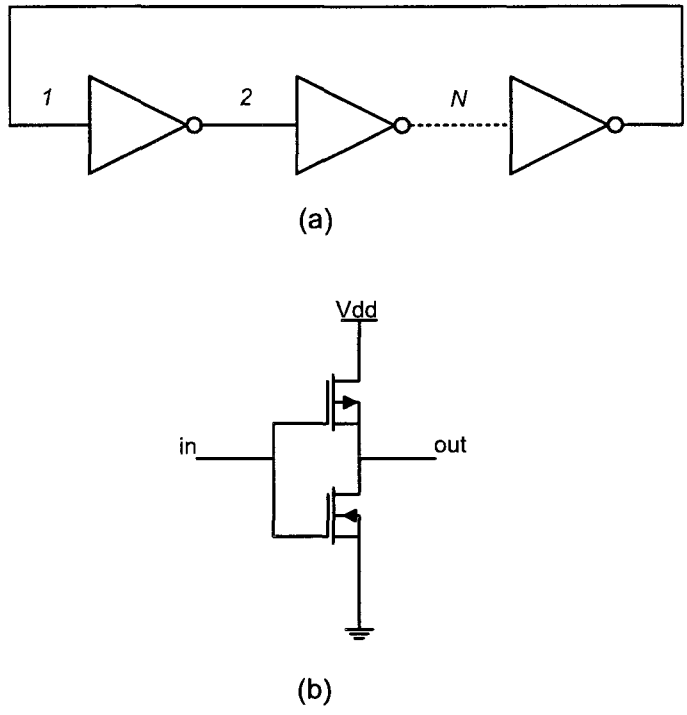


FIGURE 1.10: Ring oscillator: (a) N-stage ring oscillator (b) circuit of one inverter

the loop and will change its polarity. Supposingly that the input 1 in figure 1.10 (a) is initialized to logic '0', this value will propagate through the N inverters of the loop in $T_{osc}/2$, in which time the input 1 will change value to '1'. After another half period, $T_{osc}/2$, the value at 1 will return to '0', giving a complete period of oscillation, T_{osc}. Assuming the delay for each inverter is τ_{inv}, the duration of a half period could be determined by:

$$\frac{T_{osc}}{2} = N_{osc}\tau_{inv} \tag{1.4}$$

With this relation we could determine the frequency of oscillations given by:

$$f_{osc} = \frac{1}{2N_{osc}\tau_{inv}} \tag{1.5}$$

In general, ring oscillators are among the most used in the majority of applications (Fouzar (2005)). This is due to the fact that they are easy to integrate and they have a larger excursion range.

1.4.2.4 Comparison of the Described Oscillators

Table 1.2 compares the three different oscillators described above with respect to three characteristics: integrability, output noise and power consumption. A rank of 4 in a performance category indicates that the architecture is inherently better than the others for that category. As can be seen from this table, the LC and the ring oscillators have the lowest output noise, the relaxation and the ring oscillators are easiliy integrable, and the relaxation oscillator has the lowest power consumption.

TABLE 1.2: Characteristics of the main topologies of oscillators

Characteristic / Oscillator	Integrability	Low output noise	Low power consumption
LC oscillator	1	4	1
Relaxation oscillator	4	1	3
Ring oscillator	4	4	2

1.4.3 Main Types of Analog-to-Digital Converters

The most important characteristics in an analog-to-digital converter (ADC) for the present application are low power consumption, conversion of non-periodic signals and small size (integrability). Many types of ADCs have been developed for different applications. Some are adapted for applications of high sampling rate, others for application requiring low power consumption, and in other cases the precision of the ADC is the most important factor.

Here is a summary of the main topologies.

1.4.3.1 Parallel ADC

This type of converters work by comparing the input analog voltage to a series of different reference voltages using several comparators placed in parallel. For a resolution of n bits, there are 2^{n-1} comparators. One input of the comparator is connected

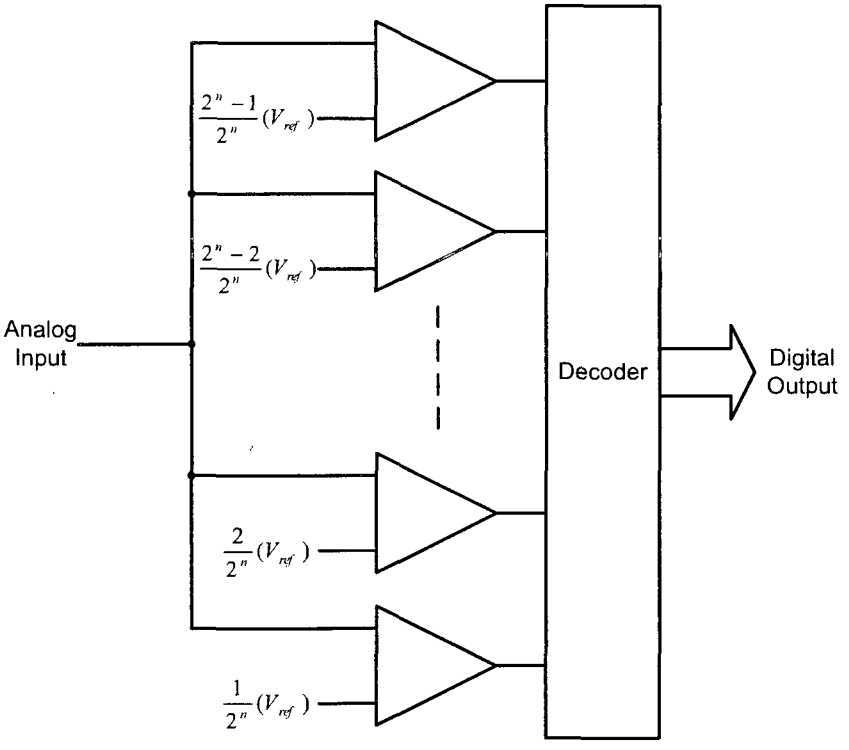


FIGURE 1.11: Block diagram of a parallel ADC

to the input signal and the other input is connected to a reference voltage as shown in figure 1.11. This reference is generated using a network of resistors acting as a voltage divider. Thus at each comparator there is a different reference voltage $V_{ref(N)}$. The output of every comparator where the input signal is greater than the reference voltage will be logic '1', while the other outputs will be at logic '0'. A decoder is connected to the output of the comparators. This decoder will convert the 2^{n-1} comparators'

outputs to a binary word of n bits.

The inconvenience of such converters are the space they occupy on a chip to obtain high resolutions, and they require identical replicas for all the comparators (Miled (2007)).

1.4.3.2 Successive Approximation ADC

SAR ADCs are known for their low speed of operation versus a low power consumption, since their architecture relies on the operation of only one comparator. In addition they are well suited for applications having non periodic inputs (Black (1999)).

The technique used here consists of approximating the analog input to binary values. An n bit successive approximation register (SAR) contains originally an initial value '0'. After that the most significant bit (MSB) takes the value of '1', and the contents of the SAR are sent to a digital-to-analog converter (DAC) that converts them to an analog value. The analog signal obtained will be compared to the input voltage. If

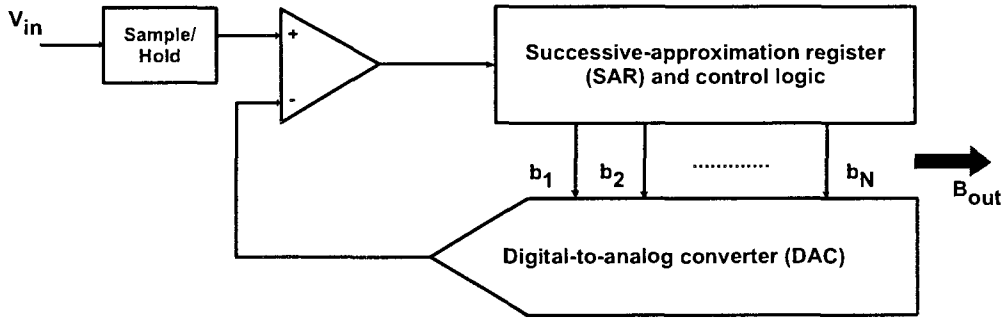


FIGURE 1.12: Architecture of a successive approximation converter

the latter is inferior to the value provided by the DAC, the bit that have taken the value of '1' will take the value of '0', and the following bit will take the value of '1'

and we redo the comparison over until we reach the least significant bit (LSB). So a given bit cannot keep the value of '1' unless the value given by the DAC is inferior to the input. As a result, we need a comparison of n stages to generate the digital value of the analog input. These types of ADCs are precise and provide often an output of parallel n-bit, and sometimes in series starting by the MSB. The architecture of successive approximation ADC is shown in figure 1.12 (Troadec (2004)).

1.4.3.3 Pipelined ADC

This architecture is adapted for high frequency circuits. Pipelining allows doing several operations at the same time. This converter is composed of several stages. The analog signal V_{in} first reaches the first stage where it is sampled and held by a sample-and-hold (S/H), while the ADC of stage 1 quantizes it to n bits, this forms the MSBs of the digital output; the n bits output is then fed to a DAC and the DAC's output is subtracted from the input and the "residue" obtained is then fed to stage 2 while stage 1 continues the same process for the following sample, and so forth until we reach stage N, for an $N \times n$ ADC. So once the latency time is achieved at the beginning, which lasts for N cycles of conversion, at every cycle we have a new digital value that corresponds to the analog input.

The major problem of this ADC is the need of a sampler/holder at each stage for which the realization is somewhat delicate, which presents the principal limitation of this architecture (Troadec (2004)).

1.4.3.4 Sigma-Delta Converter

In its basic form a sigma-delta converter consists of two modules: a mixed-signal analog/digital module that converts the analog signal into a bit stream, and a digital

filter that converts this bit stream into an n bits digital value. The mixed-signal module consists of an integrator a comparator and a single bit DAC as shown in figure 1.13.

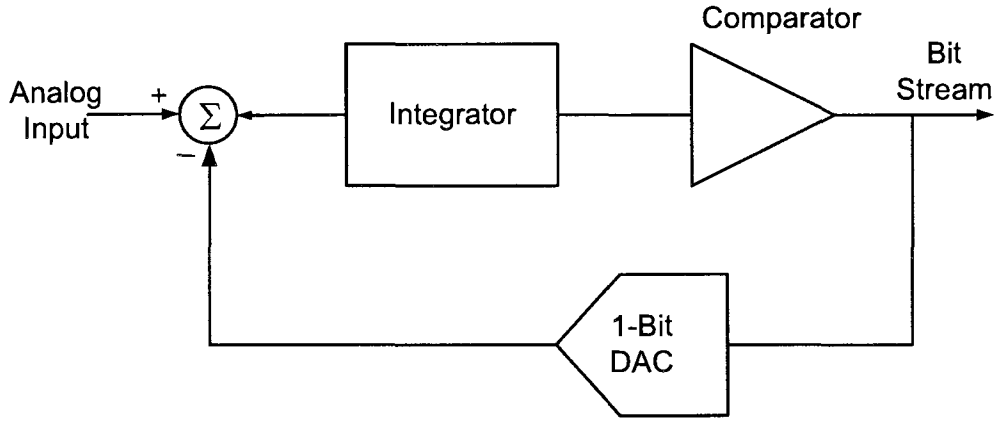


FIGURE 1.13: Analog module of a basic 1st order sigma-delta ADC

The output of the DAC is subtracted from the input signal; the resulting value is then integrated, and converted to a single bit digital value through the comparator. The resulting bit becomes the input to the DAC and goes through the loop again. This closed loop is carried out at a very high rate, in what is called "oversampling" (Black (1999)). The bit stream data is then fed to the digital filter that results in a binary digital output. The digital filter consequently has the following functions:

- Bringing the frequency of oversampling to Nyquist frequency, an operation known as decimation
- Eliminating the noise caused by the quantization.

So in other words, this filter calculates the average of the input bit stream. A limitation of this architecture is its latency, which is substantially greater than that of the other types (Black (1999)). They are not often used in multiplexed signal applications. Sigma-delta converters are not suited for high frequency signals; the

major drawback is the size of the decoder part (digital filter) which is done either by an FPGA, DSP, or a computer, so a sigma-delta converter could not be used in applications where small size is critical.

1.4.3.5 Comparison of the ADCs

At this point, we find it useful to compare the ADCs presented in this section. Table 1.3 summarizes the main characteristics of these ADCs. Also in this table a rank of 4 in a performance category indicates that the architecture is inherently better than the others for that category.

TABLE 1.3: Characteristics of the main topologies of ADCs

ADC Topology / Characteristic	Parallel	SAR	Pipelined	Sigma-Delta
Sampling Frequency	4	2	3	1
Resolution	1	3	2	4
Conversion of non-periodic signal	4	4	3	2

1.5 Recapitulation

This chapter deals with the anatomy and physiology of the human eye, and more specifically the iris and pupil. In this chapter we treat as well pathologies relevant to our work such as anisocoria; an overview about pupil size vs. ambient light is also given. Following that, an aperçu about ocular implants and prosthesis, and their development is provided. A notion about optical detectors is given. Finally, we illustrated different architectures of oscillators and analog-to-digital converters to justify our choice for the architectures.

However before proceeding to describe our work, it is important to investigate some

of the works of other laboratories working in this field, which will make the subject of our next chapter.

CHAPTER 2

INTELLIGENT OCULAR IMPLANTS

2.1 Introduction

Following the discussion about physiology and pathologies of the human eye, and the presentation of different types of ocular implants in chapter 1, we are now interested in intelligent ocular implants. The latter gives patients the ability to have a natural looking prosthetic eye, boosting their confidence.

Along this chapter we are going to describe work done in this field going from prosthetic eye movement to pupil size control.

2.2 Robotic Prosthetic Eye

Gu (2001), from the University of Alberta, have designed a robotic prosthetic eye that moves horizontally in synchronization with the movement of the natural eye. This is done by sensing the movement of the natural eye and then controlling the prosthetic eye accordingly.

They developed two generations of robotic prosthetic eye models. The first generation uses an external infrared sensor array that is mounted on the frame of a pair of eyeglasses. This sensor array is used to detect the natural eye movement and to feed the control system so to drive the artificial eye to move in synchronism with the natural one. The second generation model removes the external sensor array, and gets rid of the eyeglasses frame and uses instead the electrooculograph (EOG) signal picked up by electrodes placed on the side of one's head, carrying out the same eye

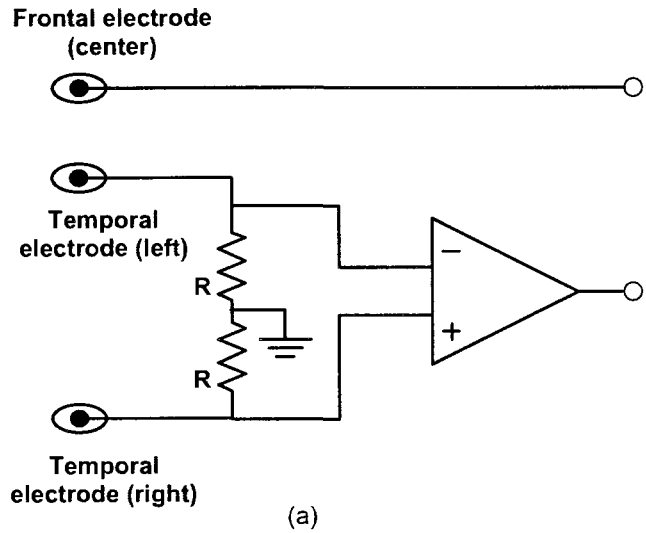


FIGURE 2.1: The robotic eye: (a) electrode configuration (second generation), (b) the artificial eye model (adapted from Gu *et al.* (2001))

movement detection and control as mentioned before.

The artificial eye is mounted onto a small servomotor to gain the movement function (Gu *et al.* (2001)). Detection of the natural eye movement is done in horizontal direction only, in both generations. Then, the motor is controlled to drive the artificial eyeball to move correspondingly, matching the horizontal movement of the natural eye. the system is depicted in fig 2.1.

2.3 Prosthetic Eye with Polarized Pupil

Young have investigated a prosthetic eye with a simulated iris painted on the front and a horizontal polarized disc at the center of the iris (Young (2007)). The center of the polarized disc is dark to simulate a pupil with a small diameter. The polarized disc is transparent, and striations are painted on its back to blend with the iris. This prosthetic eye is used in conjunction with a special pair of eyeglasses, having polarized lenses. When the eyeglasses are used, the pupil appears dilated, because they cause the entire polarized disc to be blackened. Figure 2.2 illustrates the proposed system by Young.

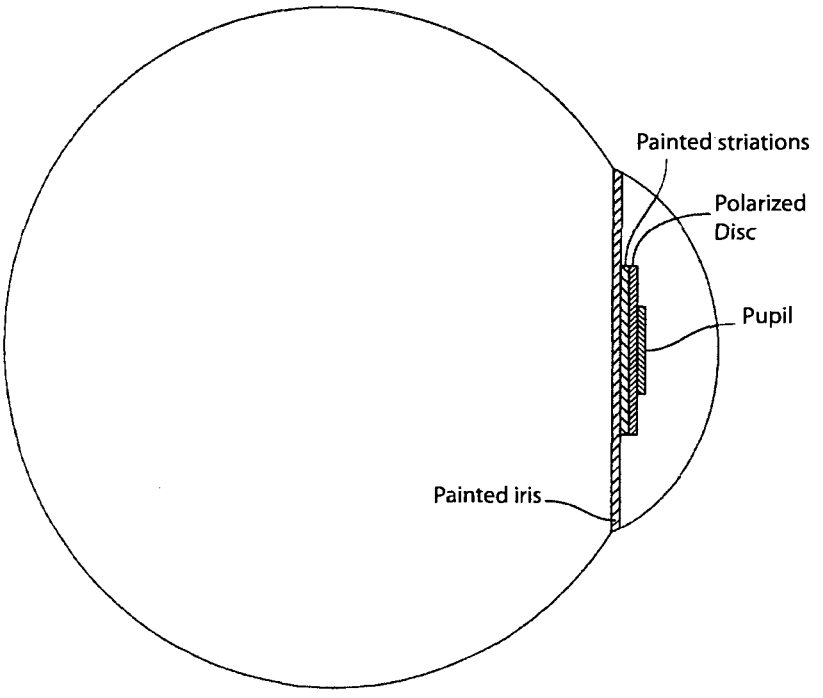


FIGURE 2.2: Cross sectional view of the prosthetic eye proposed by Young (adapted from Young (2007))

The lens that is needed to "dilate" the pupil is formed of linearly polarizing material, and has been incorporated into the patient's eyeglasses. Wearing the eyeglasses

creates the interference between the two polarized lenses (on the iris and in the eyeglasses), hence creating a larger darkened area simulating dilation of the pupil. On the other hand, removing of the eyeglasses causes the disc to lighten, showing details painted on its back, making the pupil appears to be constricted.

The issue with this system is that it does not provide automatic pupil size control, depending on the patient in its operation, hence it is not a reliable solution.

2.4 Photochromatic Dilating Pupil for Ocular Prosthetics

Friel has proposed an invention with the intent to allow for a simulation of the natural human pupil constriction and dilation (Friel (1991)).

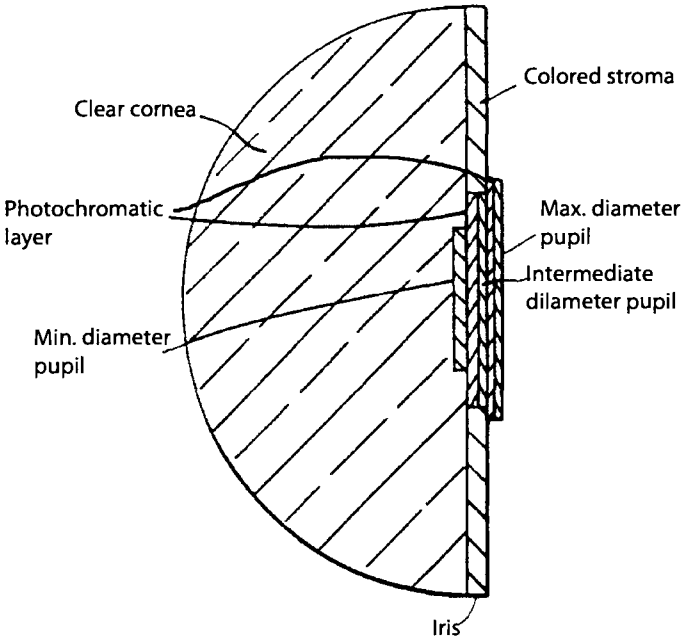


FIGURE 2.3: Side view of the ocular prosthetic proposed by Friel (adapted from Friel (1991))

This would be achieved through the use of photochromatic pigments that change their

color in response to different wavelengths of light, going from clear or transparent to opaque.

Figure 2.3 shows a side view of the ocular prosthesis. This prosthesis is comprised of an iris with a colored stroma, simulating the human iris, and three discs representing different pupil sizes (small, intermediate and large) with two discs (the two larger ones) covered by a photochromatic layer.

With bright light, the photochromatic layers will become opaque, showing only the small pupil disc and giving the impression of a constricted pupil. Upon removal from bright light, the pigments would return to their transparent state, revealing the underlying larger pupil discs, simulating a dilated pupil.

However there are some issues with the use of photochromatic layers. First they have a slow response time to light absorbtion, which is in the order of minutes, and their response is temperature dependant (Megla (1966)). Transparent photochromatic layers respond only to UV light, and do not respond to visible bright light, while photochromatic layers that respond to visible light, are not transparent in their low-light state. So with these properties, the system described by Friel do not simulate faithfully the human pupil.

2.5 Ocular Prosthesis displaying iris and pupil on a LCD

Budman *et al.* have patented an idea of an ocular prosthesis that displays an iris and pupil image on a liquid crystal display (LCD) (Budman and Stack (2003)). Their goal is to develop an ocular prosthesis having means for adjusting the apparent pupil size in response to ambient light levels. They proposed to store a plurality of iris images (dilated, constricted etc.) as data in a memory. Ambient light levels are detected by the use of a light sensor, and an image is selected based on ambient light level, and

sent to the LCD to be displayed.

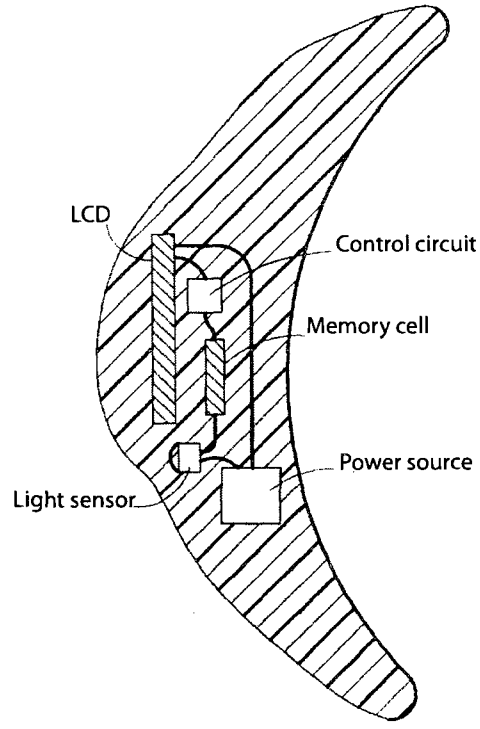


FIGURE 2.4: Cross sectional view of the eye prosthesis proposed by Budman *et al.* (adapted from Budman and Stack (2003))

The system is comprised of a color LCD positioned within the artificial eye, a memory chip coupled to the LCD, having a stack of iris images with differing pupil size to be shown, and a light sensor coupled to the memory.

Figure 2.4 shows a cross section of the prosthesis containing all the components mentioned above. The shell in front of the display is transparent so to show the iris. The memory used in this system is a non volatile programmable memory.

This system shows images of a natural iris, so in order to display accurately, the LCD should be formed of an array of very small pixels. This will make this system complex to design and fabricate, which implies it will be an expensive system and would not be available for all the patients.

2.6 Dilating Ocular Prosthesis

Schleipman *et al.* have proposed an ocular prosthetic device which can be adapted to a range of ambient lighting to simulate the appearance of a natural eye (Schleipman *et al.* (2000)). The iris image is provided with colors and patterns to reproduce the human iris. A light source is placed behind the iris image, having a series of independantly activated concentric rings to produce a size range similar to the range between a contracted and dilated pupil. The iris image has a pattern of light transmissive openings that permits light coming from the rearwardly source to pass.

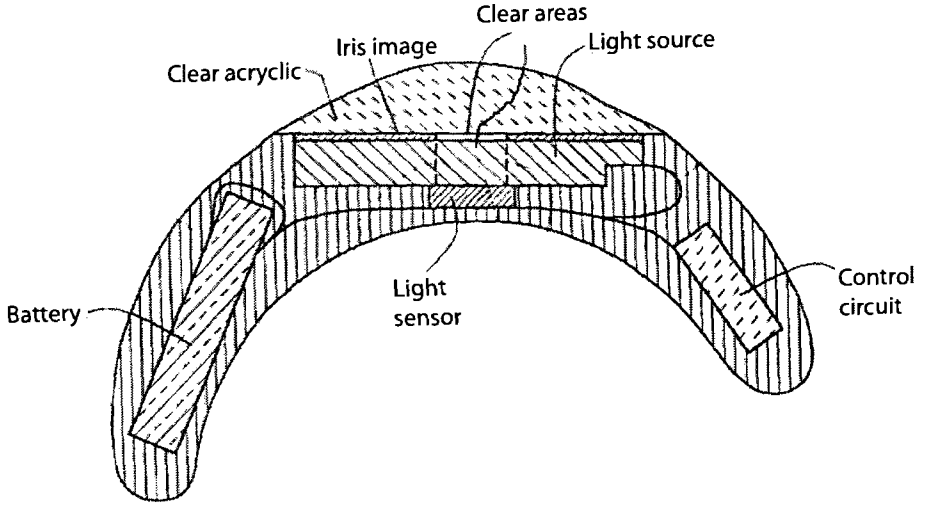


FIGURE 2.5: Sectional view of the ocular prosthetic proposed by Schleipman *et al.* (adapted from Schleipman *et al.* (2000))

The concentric rings, when activated, become darkened and could be visible through the holes in the iris image, presenting the appearence of a pupil of a size depending on the number of activated rings. On the other hand, when the rings are not activated (when they are not darkened), the iris image overlying the light source, becomes visible giving the appearence of a contracted pupil.

A light sensing device is located at the center of both the iris image and the light

source. The light sensor is connected to a control circuitry that will activate or disactivate the concentric rings according to ambient lighting. The proposed prosthetic is illustrated in figure 2.5.

However, unfortunately information about the system operation and system specifications were not provided. It is difficult to compare this system with other systems.

2.7 Recapitulation

In this chapter, different works by different researchers and universities in the domain of ocular implants and prosthetic eyes have been presented.

Since the majority of the works found in this field were patents, specific information was lacking, and the description was very general. Some of these works are not automated, i.e., they depend on the patients to operate them; others are passive optical devices, however this solution does not provide a faithful simulation of a contracting/dilating pupil. So there is a need for an inexpensive automated system that simulates a human iris and pupil faithfully. This system will be discussed in chapter 3.

CHAPTER 3

A NEW PROSTHETIC DYNAMIC PUPIL

3.1 Introduction

One of the problems with ocular prosthesis is the limited mobility of the artificial eye. This could be noticeable when the natural eye moves to extreme positions. This problem has been solved with the development of porous implants, thus allowing muscle tissues to grow into the implant, giving the prosthesis a realistic movement. The other main problem with ocular prosthesis is the fixed pupil size. This is especially a problem for patients having clear colored irides, such as green or gray.

A solution to this problem is an ocular prosthetic device that includes an automated dynamic pupil varying in size with incident light intensity. Hence, the objective of the present master thesis is to overcome the problem of post prosthesis anisocoria, by developing a prosthetic dynamic pupil to replace the static pupil that present ocular implants have. By doing so, the implant will resemble more to the natural eye.

This chapter will outline the design implementation related to the development of this system.

3.2 Discrete-Component Prototype

A prototype has been developed to validate the algorithm used in the design before proceeding to the development of the fully integrated on chip system. The prototype was developed using discrete components: a microcontroller, a photoresistive cell, transistors and miniaturized LEDs. An electrical schematic of the prototype is shown

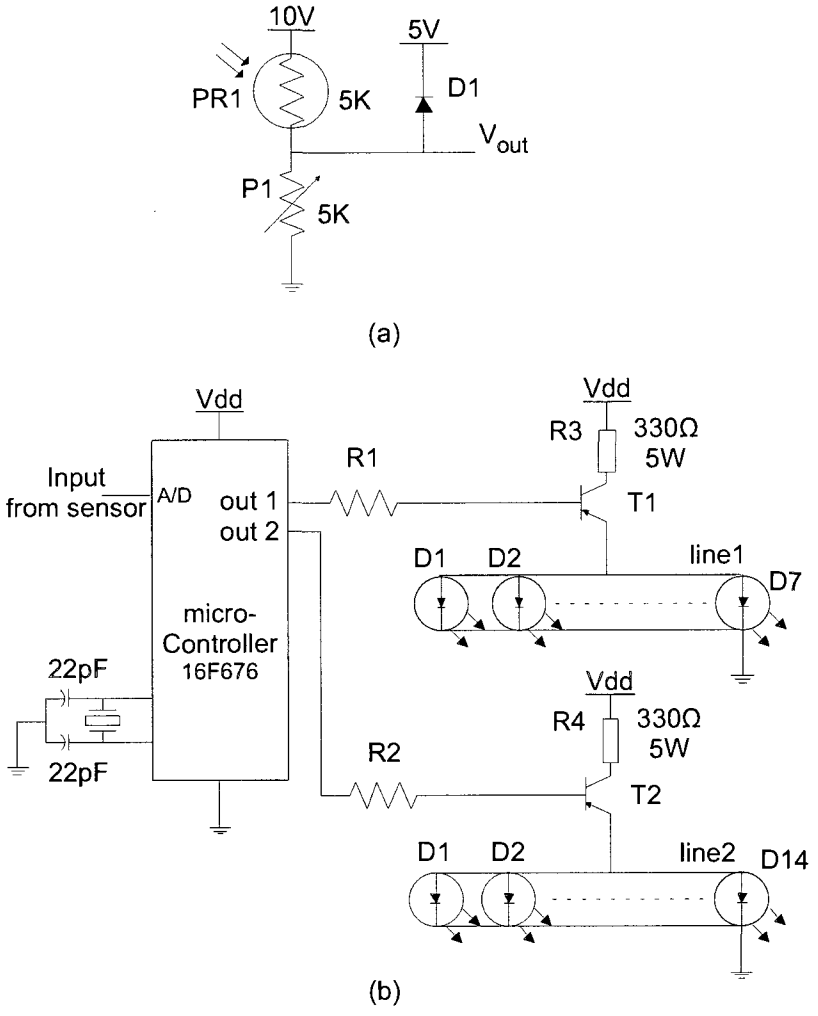


FIGURE 3.1: The electrical diagram of the prototype of the proposed system: (a) the analog part, (b) the digital part

in figure 3.1.

This design contains two parts, an analog part, shown in figure 3.1 (a), and a digital part, shown in figure 3.1 (b).

The analog part is the sensing circuit. It is composed of a photo-resistor (PR1) and a variable resistor (P1) in series between voltage supply of 10 V_{dc} and ground. When the light hitting the photo-resistor gets brighter, the resistance of the latter gets smaller and the output of this circuit (V_{out}) increases. On the other hand, with a decreased

light brightness, the resistance of the photocell PR1 increases, and V_{out} decreases.

A diode, D1, is used to clip any voltage above 5V to protect the analog-to-digital channel (A/D) of the microcontroller. The variable resistor P1 is used to calibrate the output between 0 V and 5 V.

The digital part is the controller, which consists of a microcontroller (PIC 16F676). This controller (figure 3.1 (b)) has two functions: 1) to convert the analog voltage coming from the light sensor into an 8-bit digital signal, and 2) compare this digital value with stored values in the memory and according to the result activate output 'out 1' or output 'out 2'. Out 1 activates a set of 7 LEDs through transistor T1, and out 2 activates a set of 14 LEDs through transistor T2. The LEDs used in this circuit consume a maximum of 30 mA each, so for a 5 V supply, the maximum power consumed by each LED will be:

$$P_{MAX-LED} = V_{CC} \times I_{MAX-LED} = 5V \times 0.03A = 0.15W \tag{3.1}$$

So, for ring 1, the set of LEDs will be consuming:

$$P_{MAX-out1} = P_{MAX-LED} \times 7 \times 1.5 = 1.58W \tag{3.2}$$

where 7 is the number of LEDs in line 1 and 1.5 is a safety coefficient.

For the LEDs of the ring 2, the power consumption would be:

$$P_{MAX-out2} = P_{MAX-LED} \times 14 \times 1.5 = 3.15W \tag{3.3}$$

where 14 represents the number of LEDs in line 2.

The microcontroller can supply up to 25 mA at its outputs, so with a 5 V voltage

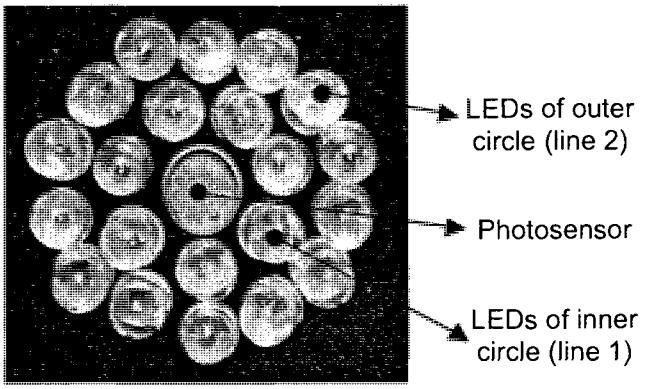


FIGURE 3.2: The prosthetic pupil developed for the prototype

supply, we get a power of 125 mW. This power is not enough to drive the output LEDs, so we resorted to the use of switching transistors to supply power directly from the power supply. By doing this, the output of the microcontroller will serve only to drive the transistors T1 and T2.

Seeing that we used standard electronic components, we assembled the control part on one PCB board, and the display part, which contains the LEDs and photocell, on another PCB board. figure 3.2 shows the prosthetic pupil developped for this prototype. In this figure, LEDs lines 1 and 2 represent two different circles forming the simulated iris, and the photosensor represents the pupil.

Test results for this prototype will be discussed in the following chapter.

3.3 Integrated Version

To further verify the proposed circuit, an integrated circuit has been implemented. A drawing of the integrated version is shown in figure 3.3. In this drawing, the shell making the white sclera and cornea is made from acrylic or glass (materials used to fabricate the classical artificial eye). The electronics represents all the circuitry controlling the display, and the display represents the artificial pupil.

So in this section we are going to describe the different modules we used in the development of this system. This system is composed of display, photosensing device, and the controller. For simplicity we will divide the integrated version into two parts: the circuits and the display.

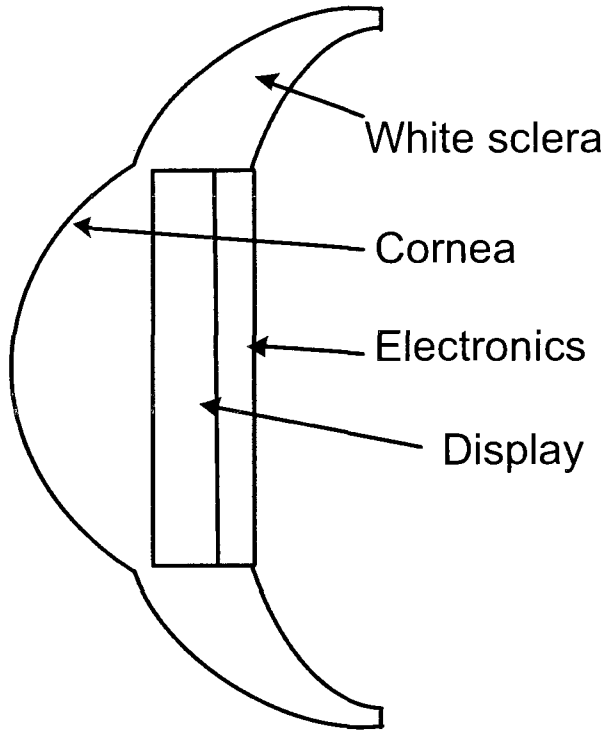


FIGURE 3.3: Drawing of the described system

3.3.1 The Circuits

The building blocks of the proposed devices include of an on chip clock generator, a delay circuit for system initialization at startup, a control circuit, and an Analog-to-Digital Converter (ADC). A block diagram of this system is shown in figure 3.4.

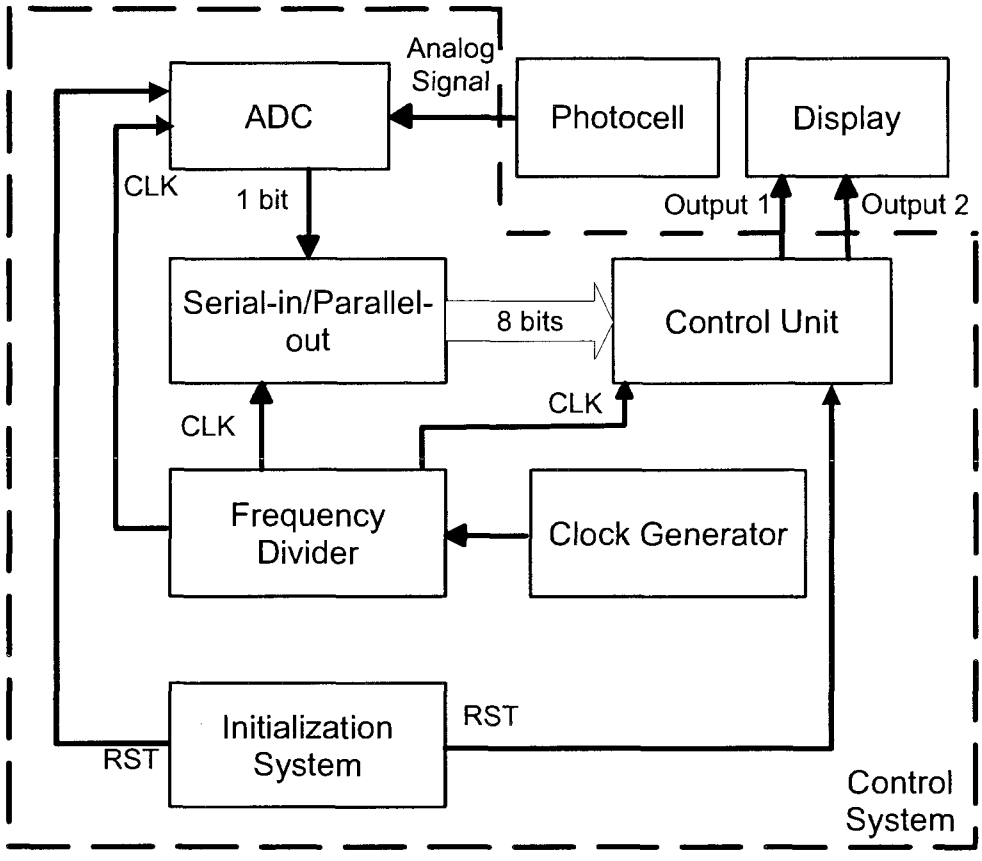


FIGURE 3.4: Block diagram of the proposed integrated system

3.3.1.1 Clock Generator

After seeing different architectures of oscillators, and exploring their pros and cons in chapter 1, we decided to choose the ring oscillator as a clock generator.

So in the proposed system we used a seven-stage ring oscillator shown in figure 3.5. The frequency of oscillation for this circuit is given by the equation 1.5. From the simulation results, the delay of inversion of each stage was measured to be $\tau_{inv} = 79.3$ ps. Replacing the variables in equation 1.5 we get a frequency of:

$$f_{osc} = \frac{1}{2 \times 7 \times 79.3 \times 10^{-12}} = 900.9 \times 10^{6} Hz \tag{3.4}$$

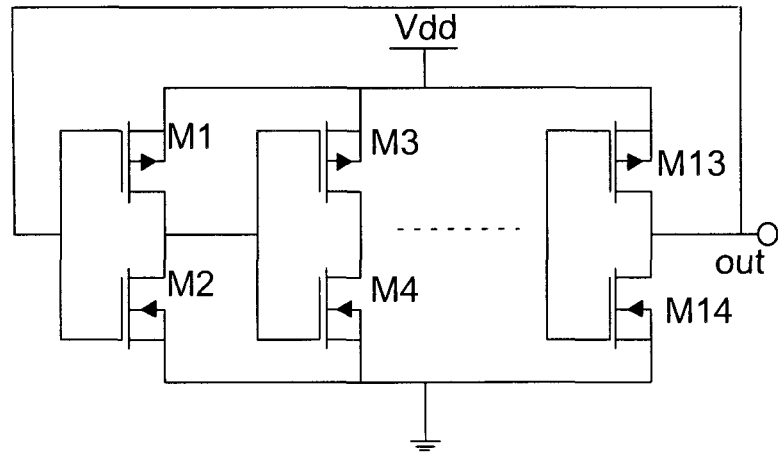


FIGURE 3.5: Schematic of the seven-stage ring oscillator

The theoretical power consumption of this ring oscillator is given by:

$$P = C_L \times V_{DD}^2 \times f \times N_{sw} \tag{3.5}$$

Where P is the dynamic power consumption, V_{DD} is the supply voltage, f is the frequency of oscillation, C_L is the load capacitance at every stage and N_{sw} is the number of switching bits.

The C_L at every stage is equivalent to the input capacitance of the inverter of the following stage. The input capacitance of a CMOS inverter is $C_{in} = \frac{3}{2}C_{oxp} + \frac{3}{2}C_{oxn}$ (Baker (2008)), where C_{oxp} and C_{oxn} are the oxide capacitance of p-channel and n-channel transistors, respectively.

By substituting these values in equation 3.5, the theoretical power consumption becomes:

$$P = (\frac{3}{2}C_{oxp} + \frac{3}{2}C_{oxn}) \times V_{DD}^2 \times f \times N_{sw} \tag{3.6}$$

So a minimum power consumption could be achieved by reducing the input capacitors of the inverters.

A frequency divider consisting of D flip-flops (DFFs) in cascade is used to bring down the frequency to 100 kHz. The DFFs were put in cascade, where the output of each DFF is connected to the input (D) of the following one, and the output of the last DFF is connected to the D of the first one. The DFF used has a master-slave architecture.

3.3.1.2 The Initialization Circuit

This element is used to initialize the controller unit at startup to start at a known state. The controller has an active low reset, so to initialize it, this circuit applies a low voltage ($0V$) at reset for a certain amount of time, after which it goes back to high ($1.8V$). In other words, the initialization circuit is a delay element having at its input a high voltage, in this case V_{dd} and at its output the delayed high voltage. The delay element used for this circuit is a current-starved delay element (Maymandi-Nejad and Sachdev (2003)) shown in figure 3.6.

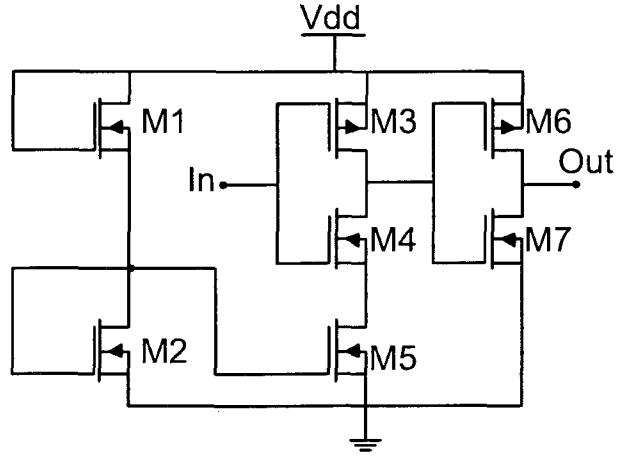


FIGURE 3.6: The delay element

As can be seen in this figure, the main unit of this circuit is the current-starved buffer formed by transistors M3 to M7. The charging and discharging currents of the output capacitance of this buffer are controlled by the current mirror composed of M2 and M5.

As soon as M4 turns on, its output capacitor starts to discharge. The discharging current is controlled by M5 which is acting as a current source. The current passing through this transistor is determined by the gate voltage of M2. The latter is in turn determined by the current passing through M2's drain. M1 controls the current flowing through M2. So the W/L ratio of transistor M1 allows to get the desired delay.

3.3.1.3 Analog-to-Digital Converter

After exploring the different architectures of ADCs used in today's circuits, we found that the best choice for our system is a successive approximation register ADC.

The ADC used is an 8-bit successive approximation register (SAR) converter from Analog Devices (figure 3.7), with a power consumption of 120 μW. This ADC has a 2.9 mm length, a 1.6 mm width and a 0.9 mm thickness, so it is easily integrated to the system. Given the low-frequency, non-periodic input signal in our current application, the SAR is the logical architecture choice.

This ADC is connected directly to the photocell, so it converts the analog output of the latter into digital data in order to be compatible with the digital control circuitry.

The conversion process and data acquisition are controlled by the $\overline{CS}$ and the clock. The input signal is sampled on the falling edge of $\overline{CS}$, and conversion is also initiated at this point as well. The needed reference voltage (V_{ref}) is taken internally from

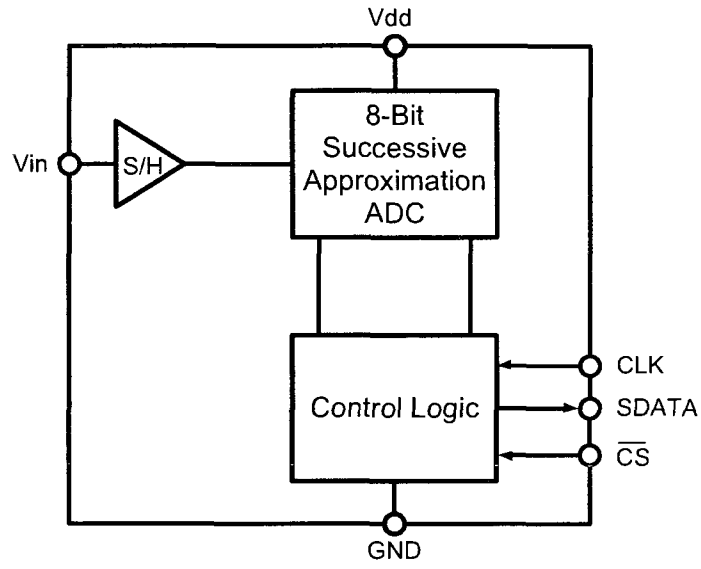


FIGURE 3.7: Block diagram of the utililised ADC

V_{DD}, allowing the widest dynamic input range for the ADC. Hence, the analog input range is from 0 V to V_{DD}. $SDATA$ represents the serial output of the ADC. The reason for which we chose an ADC having a serial output is that it has less pins and thus is smaller than parallel output ADCs.

3.3.1.4 The Controller Unit

The controller unit is the main module in the electronics part. It controls the contraction and dilation of the prosthetic pupil. The controller input is connected to the ADC output. The controller has an 8-bit input, and since the ADC has a serial output, a serial-in/parallel-out register have been implemented to connect the ADC and the controller together (figure 3.8). The data coming from the ADC contains information about ambiant light. The controller then transforms this information to light intensity and controls the prosthetic pupil according to Table 1.1. The controller provides three levels of animation for the prosthetic pupil, going from fully contracted to fully dilated. So the controller should have two outputs to achieve such resolution,

going from '00' to '11'.

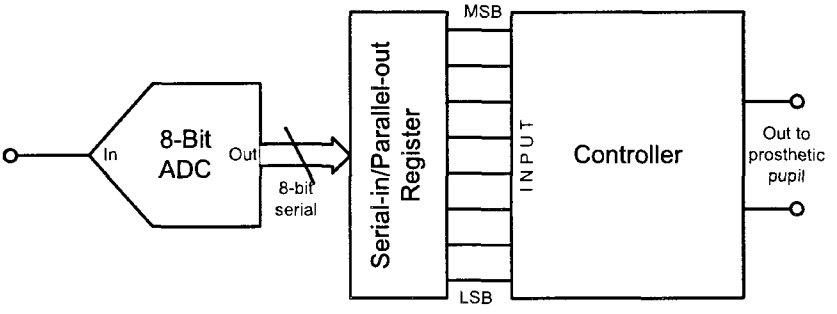


FIGURE 3.8: The controller and ADC

Since the control unit is only detecting for two values and the display is providing three levels of animation, in this version of the system, two comparators could be used instead of an ADC; however we decided to use an ADC so we could extend the animation of the display to n levels. Figure 3.9 shows a block diagram with two comparators replacing the ADC.

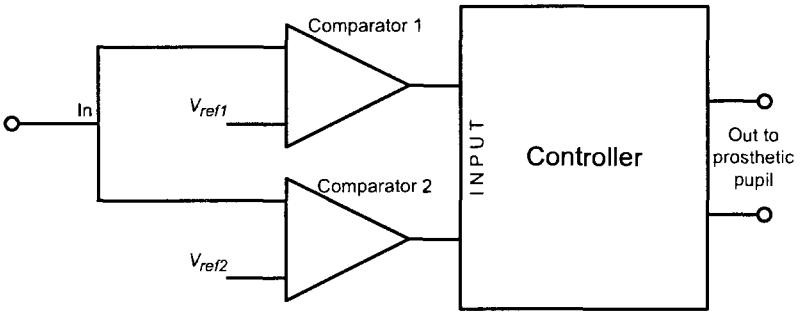


FIGURE 3.9: The controller and two comparators replacing the ADC

In the diagram in figure 3.9, comparator 1 will compare the voltage coming from the photodiode to a reference voltage (V_{ref1}) equivalent to an illuminance of 1 lux, and comparator 2 will compare the voltage coming from the photodiode to another reference voltage (V_{ref2}) equivalent to an illuminance of 316 lux.

The controller was implemented and tested in VHDL. The implemented algorithm,

compares the input to values equivalent to the luminance in Table 1.1, then it controls the prosthetic pupil according to the luminance range. The algorithm was then synthesized using Design Vision (Synopsys, Inc.) and a netlist was generated. The physical circuit was then created using the place-and-route tool SoC-Encounter (Cadence). In the implementation and testing of the controller, we followed the digital design flow provided by the CMC Microsystems shown in figure I.1 of appendix I.

The algorithm used in the design of the controller goes as follows:

```
if (IN > 316 lux) then
     OUT1 = 0
     OUT2 = 0
     elsif (1 lux < IN < 316 lux) then
          OUT1 = 1
          OUT2 = 0
          else
            OUT1 = 1
            OUT2 = 1
endif;
```

So for bright light, i.e., greater than 316 *lux*, the two outputs of the controller are shut down leading to a display simulating a contracted pupil. In room light (second case), only output 1 of the controller is on, activating the first line of the display. And in dim light, the two outputs of the controller are on leading to a display simulating a dilated pupil.

The first reason behind choosing the digital approach over the analog is its ability to provide several levels of animations for the display without any complex or added circuitry. The second reason is the capability to generate a square wave output with

a controlled duty cycle in order to reduce the display activation time, therefore its energy consumption.

The controller outputs are provided as a square wave having a frequency of 20 kHz and a duty cycle of 20%. The Energy consumed by the display would become: $E_{Disp} = 20\% \times T \times V_{DD} \times I_{DD}$, hence reducing 80% of the energy it consumes.

3.3.1.5 The Display

The use of the liquid crystal technology would, of course, give a more realistic prosthesis, so we decided to contact several specialized companies, located in Taiwan, Germany, the USA and Canada for that matter; however we didn't get positive responses from them, while some said they could not fabricate LCDs that small (the size of a human iris), others said they could, however they would do it only for very large quantities. Hence, with the technology present today, the development of an LCD the size of a human iris would be very expensive, so a compromise have been made, and the prosthetic pupil was developed using LEDs for the time being. The display for the integrated version is built using 114 miniature LEDs. Each LED has a size of 1.0 mm x 0.5 mm. These were disposed in a circular layout, forming a display having a diameter of 12 mm reproducing the human iris. At the middle of this display, a region having an area of 4 mm^2 will not be affected by the intensity of ambient light; the light sensor will be placed in this area. The space that varies depending on light quantity is a ring having an interior diameter of 2 mm, and a total diameter of 12 mm.

The light sensor is a photodiode (TDK, Garden City, NY) with a size of 1.5 mm x 2 mm, a spectral sensitivity area between 350 and 750 nm and an illuminance range between 0 and 75,000 Lux. Figure 3.10 shows the spectral response of the used photodiode, and compares it with the spectral response of the human eye.

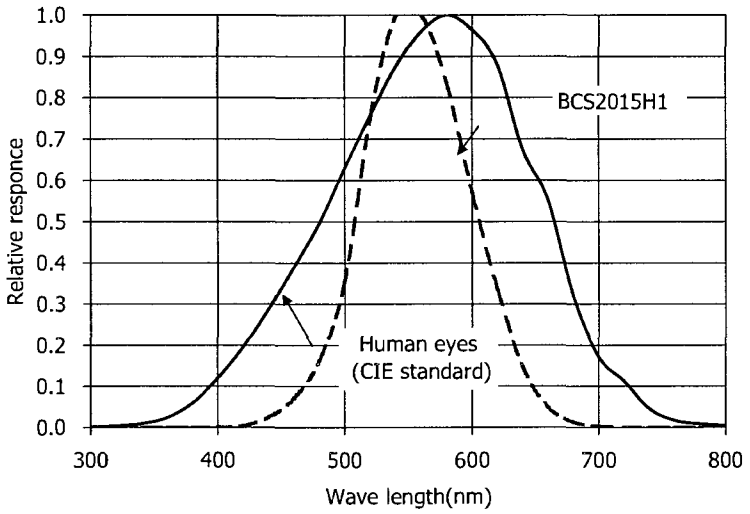


FIGURE 3.10: Comparison of the spectral responses of the human eye and the used photodiode (From Digikey datasheets)

The LEDs form two independent rings, giving three levels of animation, as mentioned above. These two rings are controlled by the controller's two outputs. The mixed use of solar cells and photosensors would have been a good idea to generate power and recharge the battery, however seen the size of the prosthesis and the photocell, a solar cell would have to be very small to get integrated in this system, hence would not generate enough power to supply the system neither to charge the battery.

The PCB layout of the system is done using PADS Layout from Mentor Graphics Corporation. Figure 3.11 (a) shows a drawing of the display, and its layout is shown in figure 3.11 (b).

This system would be inserted into an already fabricated ocular prosthesis, and would be held using biocompatible epoxy. So the system would not be subjected to the high temperature of the processing stage.

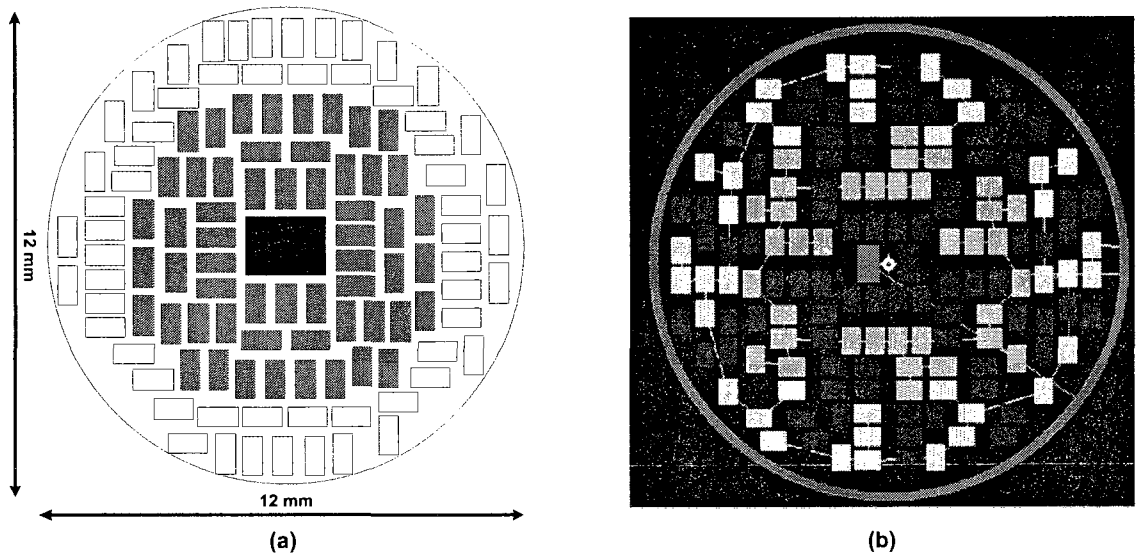


FIGURE 3.11: The integrated version display: (a) a drawing of the display, and (b) its layout

3.4 Power Consumption

The power consumption of the electronics part of this system is 520 μW (289 μA for a voltage of 1.8 V). The power consumption of a commercial LCD display is 0.11 W/in^2 for a voltage of 110 V, which gives a current of 1 mA/in^2. In this system the display is circular with a diameter of 12 mm and an area of $A_d = 113\ mm^2$. The power consumption of this display is 0.175 mA. The complete system power consumption is 463.8 μA.

3.5 Recapitulation

In this chapter, a complete system acting as a dynamic prosthetic pupil, to overcome the problem of post-prosthetsis anisocoria have been described. This system simulating the human iris, has a circular form with a diameter of 12 mm, and a thickness of 6 mm. This system is composed of a controller, a display and a photosensitive cell. The

controller is implemented in 0.18 μm CMOS technology; the display is constituted of 114 mini-LEDs each having a size of 1.0 mm x 0.5 mm forming the circular display; and the photodetector is a commercially available photodiode having a size of 1.5 mm x 2 mm, a spectral sensitivity area between 350 and 750 nm and an illuminance range between 0 and 75,000 Lux.

The role of the controller is to take light information from the photocell, transform it to light intensity (lux), compare it with stored values and finally to control the display suitably so as to give the appearance of a contracted pupil in strong lights and dilated pupil in dim lights.

CHAPTER 4

RESULTS

4.1 Introduction

In the previous chapter we presented the proposed rehabilitation system. This chapter presents the results obtained following simulations and experimental testing.

Section 4.2 presents results obtained from the experimental validation of the prototype. Section 4.3 presents the results obtained from the tests of the VHDL code on the prototyping board. In section 4.4 we present some precautions we took while doing the layout of the circuit. Section 4.4.1 will be dealing with the post-layout simulation results of the integrated version, and section 4.5 shows the experimental results of the integrated version.

4.2 Prototype Experimental Validation

The first step in the experimental verification included a prototype implementation. The developed prototype was assembled on an in-house PCB using discrete components: a microcontroller, a photoresistive cell, transistors and LEDs. The schematics of the control circuit is shown in figure 3.1. The prosthetic pupil of this prototype is shown in figure 3.2. The prototype was tested in different lighting conditions: dim light, room light, and bright light. Results for these tests are illustrated in figure 4.1.

For bright light, neither line 1 nor line 2 are active. For normal lighting, only line 1 is active, while both lines are active for dim light. So by doing this, the LEDs are simulating a pupil that contracts in high density light and dilates in low density light.

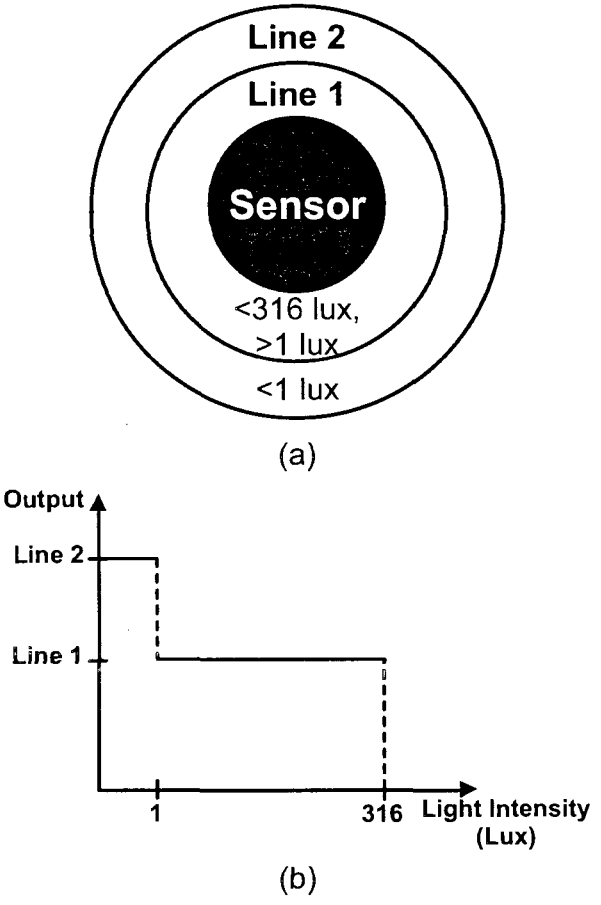


FIGURE 4.1: The prototype test results: a diagram (a) and a graph (b) illustrating the prototype output

With these results we were able to prove that the concept experimentally works. To further verify the proposed circuit, an integrated circuit has been implemented.

4.3 FPGA Prototyping Board

Before proceeding to the implementation of the IC and the post-layout simulation, the VHDL code implementing the control module was further tested on a FPGA prototyping platform from Fusion, Actel shown in the figure 4.2. So the VHDL code was synthesized and implemented on the FPGA platform in order to be tested. At the

input we used a photodiode (the same used for the integrated version) that generates an output voltage going from $0V$ to about $650mV$ depending on light intensity, and at the output we had two on-board LEDs each representing a ring of LEDs as represented in figure 4.1. Since the controller is digital, an ADC had to be employed. We used the programmable Successive Approximation Register ADC offered by the Fusion family. This ADC can support 8-, 10-, or 12-bit modes of operation. An analog module called the "Analog Quad" is placed at the input of the ADC, this module, also unique to the Fusion family, contains four blocks: Voltage Monitor, Current Monitor, Gate Driver, and Temperature Monitor. Since the output of the photodiode is a voltage, we were only interested in the Voltage Monitor block. This block contains a two-channel analog multiplexer, which allows the incoming analog signal to be routed directly to the ADC, or allows the signal to be routed to a pre-scaler circuit before being sent to the ADC. Since our input signal is already compatible with the ADC input range, we routed the input directly to the ADC. We configured the ADC to operate in the 8-bit mode. A flash memory is used to program the ADC. This memory is generated using the "Flash Memory System Builder" offered by the Fusion technology.

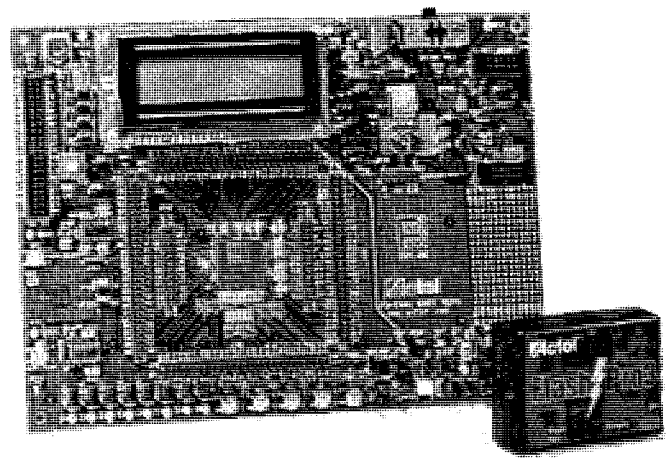


FIGURE 4.2: The Fusion development kit (Source: www.actel.com)

A clock generator has also been employed using the internal "Oscillator - RC" block.

This block is an on-chip free running clock source.

Once the FPGA was programmed, we connected the photodiode to the input, and tested the VHDL code in different lighting. The results were similar to those obtained from the first prototype.

4.4 Implementation of the Full Custom Version

Following the functional design, we proceed now to the full custom design and implementation. This task is very important when it comes to the operation of the circuit. When drawing the layout we should take into consideration the minimization of the effects of certain aspects such as parasitic resistors and capacitors, component mismatch, and noise. Along this section we will provide the results of the post-layout simulations, then we will present some precautions we took while doing the layout of the circuits.

4.4.1 Post-Layout Simulation

The IC of the full custom version was implemented in a CMOS 0.18-μm technology from TSMC, with a supply voltage of 1.8 V. This chip has a total layout size of 1.25 mm $\times$ 1.05 mm.

The first step during a circuit verification is the validation of its operation module by module, then verify the operation of the complete chain. So we will start by testing the clock generator first, then we will test the delay circuit, then the controller, and finally we will connect the different modules together and test them as one module.

4.4.1.1 The Clock Generator Module

The layout size of this module is 95 μm × 57 μm. The layout is shown in figure 4.3.

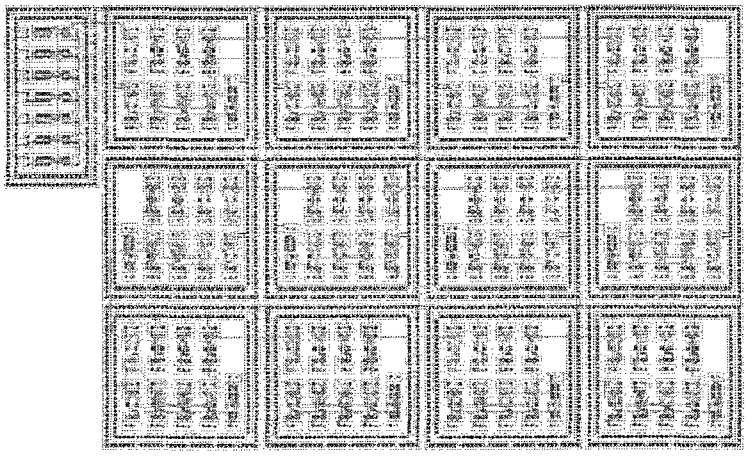


FIGURE 4.3: Layout of the clock generator

This drawing contains the layout of the ring oscillator along with the frequency divider. All blocks are surrounded by two guard rings connected respectively to VSS and VDD.

Post-layout simulations of this module resulted in oscillations having a frequency of about 180 kHz. The results of the post-layout simulation are shown in figure 4.4.

4.4.1.2 The Delay Module

The layout size of the delay circuit is about 23 μm × 15 μm. The layout is illustrated in figure 4.5.

This module (figure 3.6) was used to initialize the system at startup by applying a logic '0', at the reset of the controller, for a period of 4 μs after which a logic '1' is applied. So at the input of the delay module VDD is connected and at the output we have a delayed VDD.

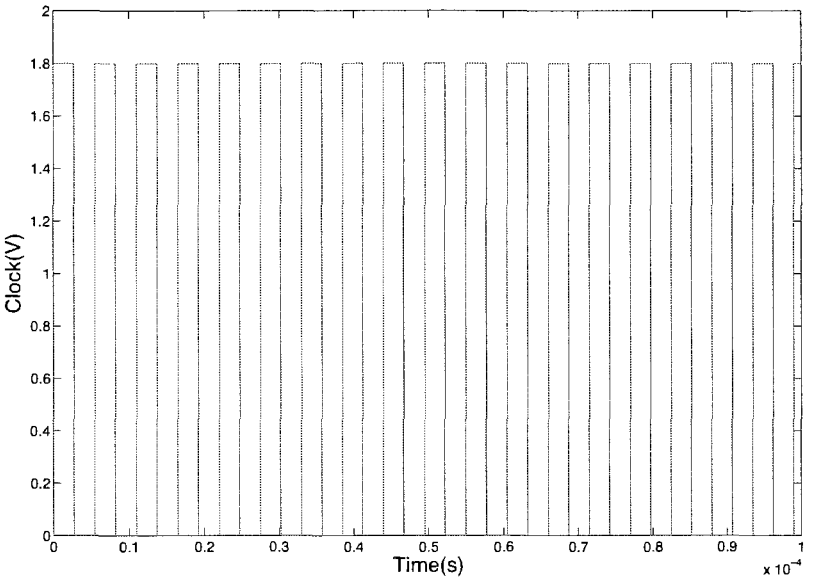


FIGURE 4.4: Post-layout simulation results of the clock generator

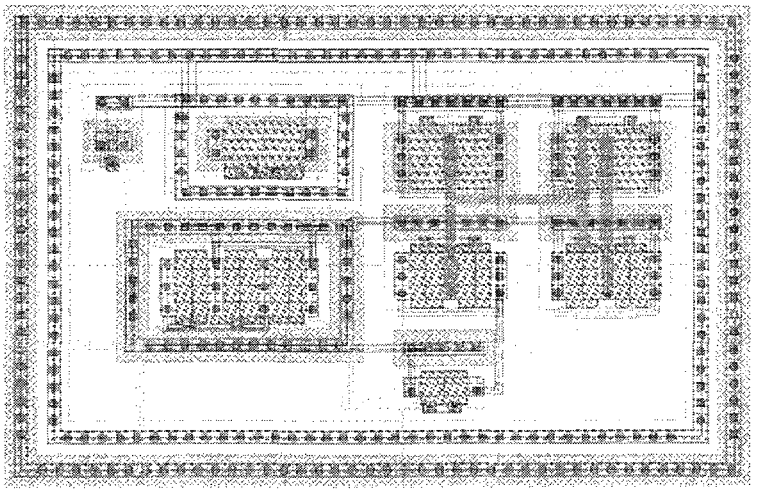


FIGURE 4.5: Layout of the delay circuit

Figure 4.6 illustrates the post-layout simulation results of this module.

The input, VDD, is switched on at 0 s along with the system; the output is switched on 4 μs later.

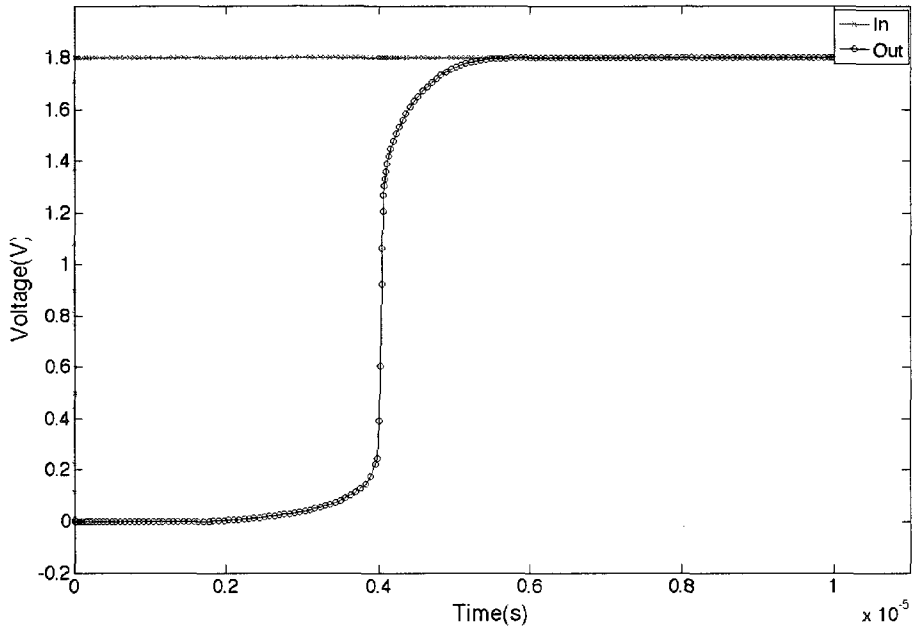


FIGURE 4.6: Post-layout simulation results of the delay unit

4.4.1.3 The Controller Module

This module is an all-digital controller, so we used the digital blocks provided by the "artisan" library from TSMC. The layout of the control module is shown in figure 4.7.

At the input of the controller a digital signal coming from the ADC is applied, this signal contains information about light intensity. The output of this controller is consisted of a two-bit word controlling a two-line LED display, similarly to the prototype.

So as explained in chapter 3, the controller output is provided as two square waves having a frequency of 20 kHz. The output of this module is illustrated in figure 4.8.

In this graph we can see the two outputs of the controller: line 1 and line 2. The input is a signal representing the ambient light. The impulses in the outputs indicate

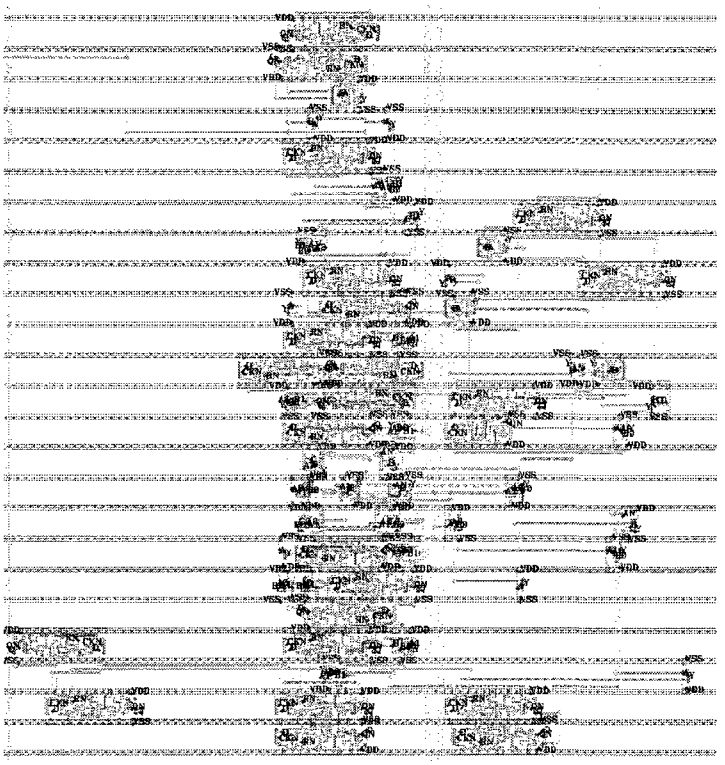


FIGURE 4.7: Layout of the control module

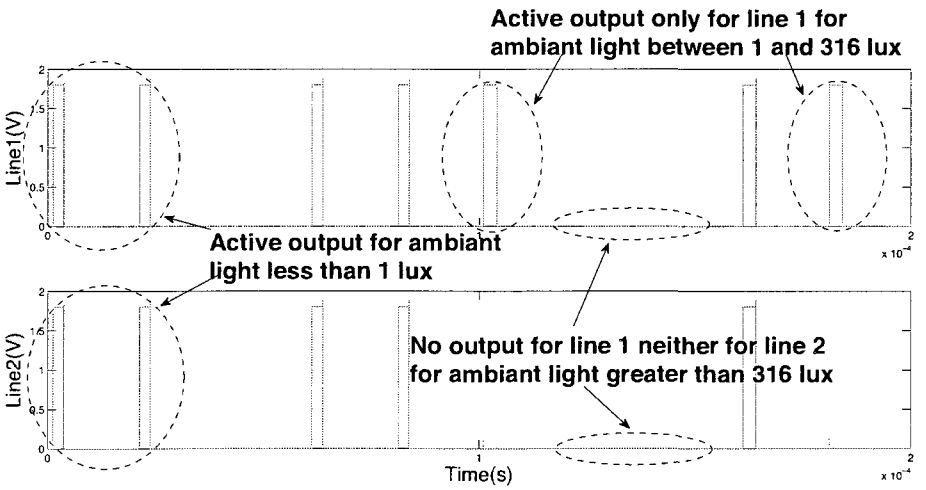


FIGURE 4.8: Post-layout simulation results of the control module

an active output. Line 1 is active alone for an ambient light between 1 lux and 316 lux, line 1 and line 2 are active together for an ambient light below 1 lux, and there is no output for an ambient light greater than 316 lux. Line 2 is never active alone because it represents the outer line of the iris.

4.4.1.4 The Complete Integrated Circuit

After seeing that every module works correctly alone, now we need to connect all the modules together and verify the operation of the complete chain. Once all the modules connected together, we added pads and bonding pads from the TSMC "tpz973g" library provided by CMC Microsystems. The complete IC has an area of 1.25 mm × 1.05 mm.

The layout of the complete chain, with all modules connected together is shown in figure 4.9. In this figure the pads appear to be empty boxes, that is because the "tpz973g" library is a Virtual Silicon Technology (VST) library, i.e., all cells in this library are black-box cells giving access only to the input/output behavior and their physical dimension.

The system was tested as a unity, with a supply voltage of 1.8 V. The results were identical to the results of each module alone. The circuit was simulated with different resistive and capacitive loads at the output.

The load impedance Z is equal to:

$$Z = R \,//\, \frac{1}{j\omega C} = \frac{R \times \frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \tag{4.1}$$

with an output frequency of 20 kHz, $\omega = 2\pi \times 20\ kHz$, and a load of $R = 1\ k\Omega$ and $C = 50\ pF$ we have an impedance of:

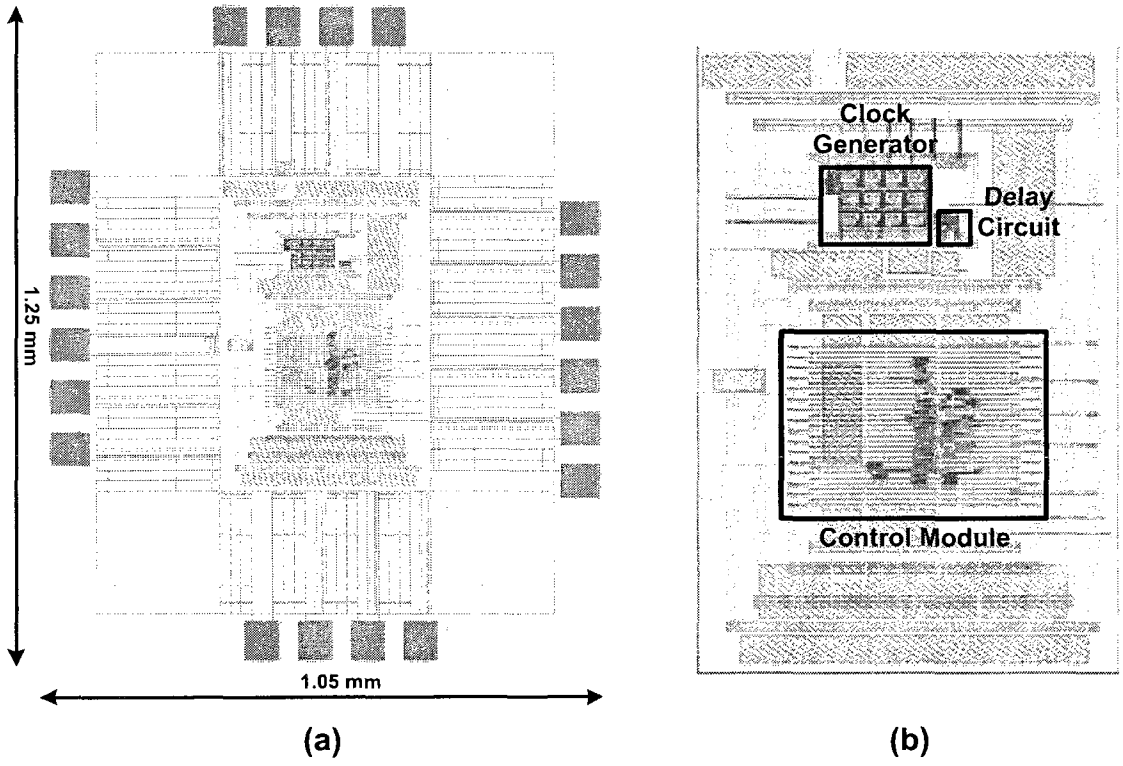


FIGURE 4.9: Layout of the complete integrated circuit (ICFPMMRW): (a) the complete layout with pads, and (b) detailed different modules

$$Z = 0.025 - j155.22 \tag{4.2}$$

At this output load we had a signal attenuation of 8.3%.

4.4.2 Precautions to Minimize Parasitic Elements

We followed some basic rules to minimize the additional extraction of parasitic resistors and capacitors in our layout.

As a rule of thumb, we avoided to draw in a single segment a transistor with a very large W. It is preferable to divide the transistor in smaller parallel units. We do this

in order to reduce the parasitic resistive effect of the poly-Si that forms the transistor's gate, as well as to reduce the value of the depletion capacitors at the source (C_{sb}) and at the drain (C_{db}) of the transistor by a value of about $(n+1)/(2n)$, where n is the number of the parallel elements.

Also we should maximize the number of contacts that allow the connection of the drain (D) and source (S) of the transistor to another element of the circuit. The same principle applies to vias that connect metals of different layers. In fact, every contact and via contains a parasitic resistor and is limited to a certain current density. So by increasing the number of contacts and vias for a given area, we reduce the resulting equivalent parasitic resistance and the current density.

When it comes to routing the interconnexions, we should avoid the use of long segments of metals, because it generates parasitic resistors and capacitors which value depends on the length and width of the metal.

Finally we should avoid to route a signal using the layer poly-Si, since it is a lot more resistive than metal layers. So in our layout, we used metal M1 to M6 to route the signals, and we used the poly-Si only to draw the gates of the transistors.

4.4.3 Precautions to Minimize Noise

In every microelectronic circuit, coupling noise coming from within the chip presents problems. To reduce the effects of the injection noise coming from the substrate, we isolated the modules from each others using two guard rings, p^+ connected to VSS and n^+ connected to VDD and lying on a n-well.

Finally we should mention the crosstalk noise. Between two segments of metal, there exists mutual capacitances and inductances that causes signals from one segments to interfere with the other segment. So while doing the layout, we minimized the effects

of crosstalk by adding more space between two adjacent parallel segments within a certain area.

4.5 Experimental Results

A microphotograph of the fabricated chip is shown in figure 4.10. The die has a total area of 1.3 mm^2.

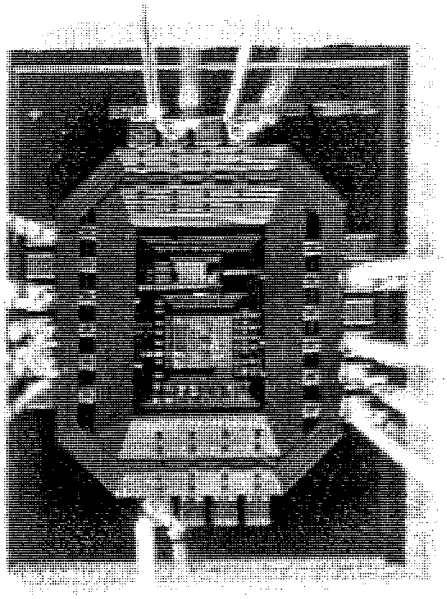


FIGURE 4.10: Microphotograph of the fabricated chip

Test configuration was realized to collect the clock signal and the two controller outputs. The testbench consisted of a SA-ADC, the chip, a light sensor, a power supply and an oscilloscope. Since the clock signal was generated on-chip, we do not need a function generator. The testbench configuration is illustrated in figure 4.11.

When we supplied the system, first we measured the clock signal, we visualized a signal having an amplitude of 1.76 V and a frequency of 172 kHz. The measured signal is shown in figure 4.12.

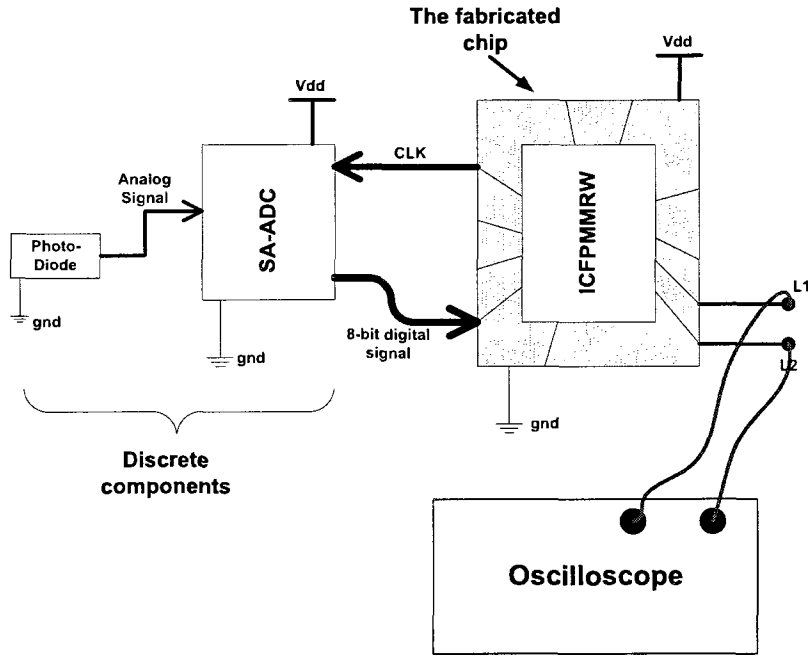


FIGURE 4.11: Testbench configuration

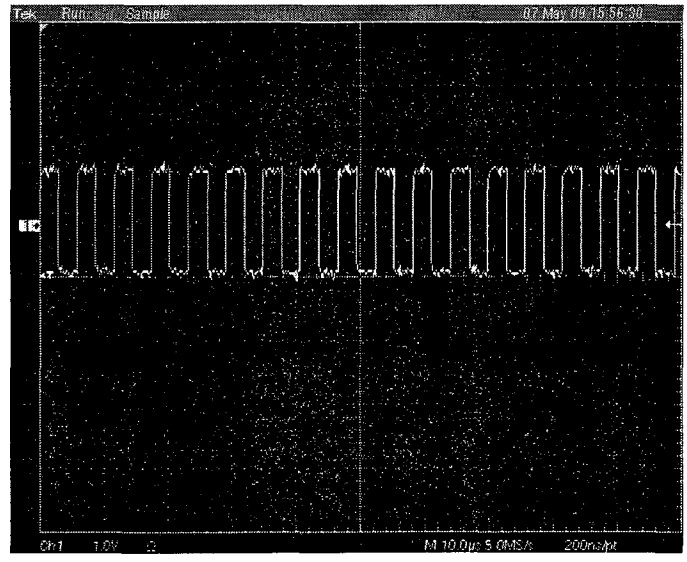


FIGURE 4.12: Measured clock signal (the frequency of the signal is 172 kHz)

The chip was tested as shown in figure 4.11, and the results were similar to the post-layout simulation results, taking into consideration the four leading zeros coming from

the ADC in front of the data bits. We started testing the chip for very dim light, i.e., 0 V analog input, we measured at the outputs an active signal, as expected, which translates to a fully dilated pupil. Then we tested for bright light, i.e., 600 mV analog input, and we measured 0 V at the two outputs, also as expected, which translates to a fully constricted pupil.

Figure 4.13 shows the measurement of obtained for dim light, both outputs are active.

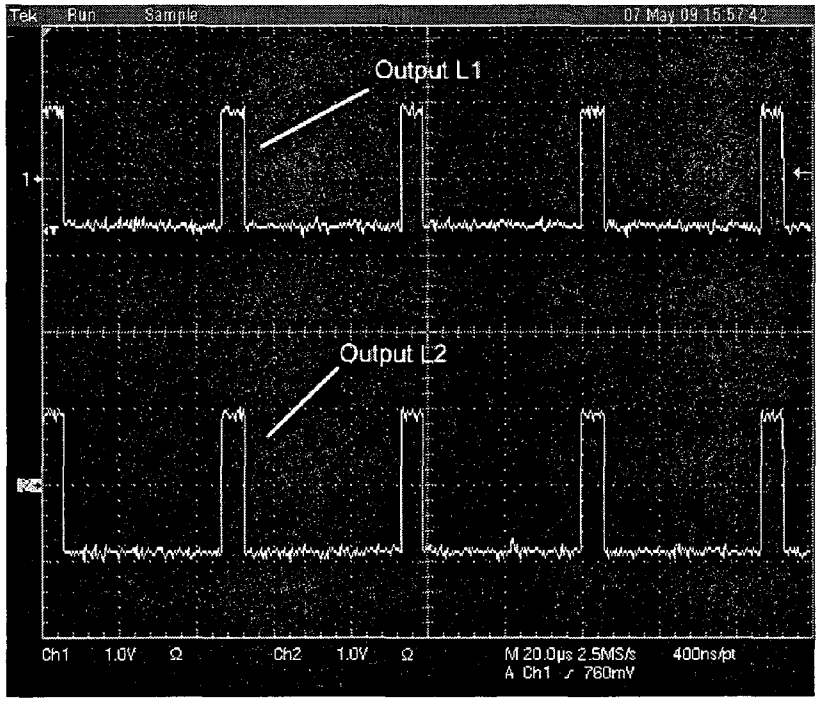


FIGURE 4.13: Measured outputs for dim light: L1 and L2

The measured outputs when active, represent two square waves with a frequency of 21 kHz and a duty cycle of 13.5%, each.

Figure 4.14 shows measurement obtained for room light, i.e., light intensity between 1 and 316 lux. We had an active output at L1, and 0 V at L2.

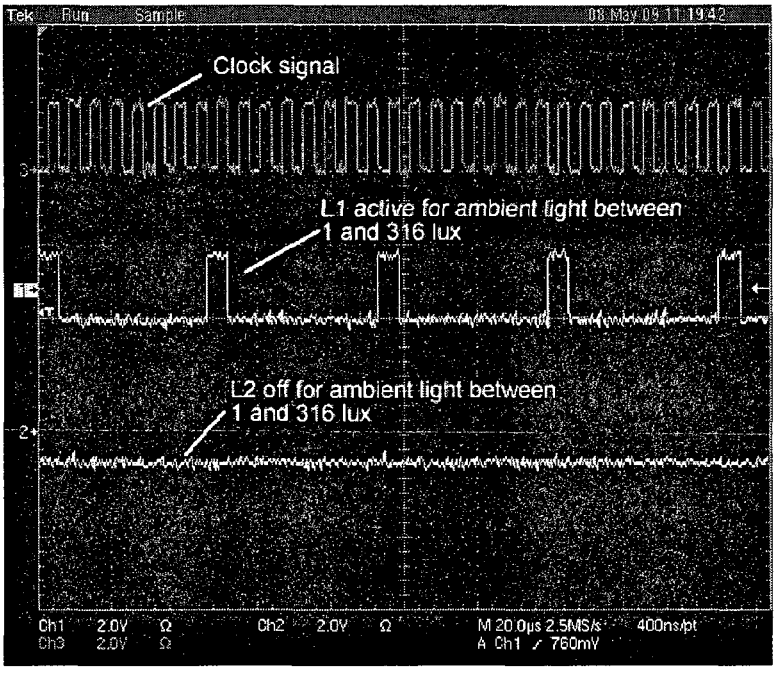


FIGURE 4.14: Measured outputs for room light: clock signal, L1 and L2

4.6 Comparison Between Experimental and Post-Layout Results

In order to quantitatively validate the fabricated chip, we compared different parameters of our post-layout simulation results with measurements. The parameters we compared are the clock's frequency, and the output's duty cycle and frequency.

TABLE 4.1: Simulated vs. measured parameters

Parameter	Simulated	Measured	|Error %|
Supply voltage	1.8 V	1.8 V	N/A
Clock voltage	1.8 V	1.76 V	2.2 %
F_{CLK}	180 KHz	172 KHz	4.4 %
Output voltage	1.8 V	1.76 V	2.2 %
F_{OUT}	20 KHz	21 KHz	5 %
Duty cycle (out) %	20 %	13.5 %	32.5 %

As seen from Table 4.1, a very good agreement is obtained between simulated and measured parameters. However, there still is a small percentage of error between simulated and measured values, this is due to process variation, the addition of output buffers, and parasitic capacitance from pads.

4.7 Recapitulation

In this chapter we described tests performed on the prototype and integrated controller presented in chapter 3, and the results of these tests were presented. We mentioned also the precautions we took while doing the layout of the circuit to minimize the effects of noise and parasitics. We started first by the experimental validation of the developed prototype, we tested it with different lighting conditions, we visualized an animated pupil. Following that we implemented our VHDL code on a FPGA testing board from Actel, and we tested it using a photodiode, and the results was similar to those obtained from the prototype. After that we mentioned the post-layout tests and results of each module constituting this system. Then, we addressed the experimental testing and results of the fabricated chip. Finally, we compared the measured results to the simulated results and found them to be in good agreement.

CHAPTER 5

LOW POWER ADC FOR BETTER INTEGRATION

5.1 Introduction

In chapter 4 we illustrated the operation of the proposed system. However the major drawback of this circuit is that it contains an off-chip ADC, causing it to occupy a larger space, and consuming more power.

For this purpose, an improvement fixing this drawback will be presented in this chapter, and simulation results will be illustrated in order to validate the circuits used.

5.2 The Integrated ADC

The designed and implemented ADC is an 8-bit neuromimetic topology, originaly developed by Yakoub *et al.* (2009), and we adopted it for our proposed system. This Neuron Cell ADC (NC-ADC) is inspired from the operation of a neuron. A block diagram of this circuit is illustrated in figure 5.1. The following is a description of the main building blocks of this ADC, namely the neuron cell, the calibration circuitry, and the pulse counter.

1. *The Neuron Cell*

This module is similar in function to the human neurons in the way that it takes current (ions) at the input and it generates pulses (action potentials - APs) at the

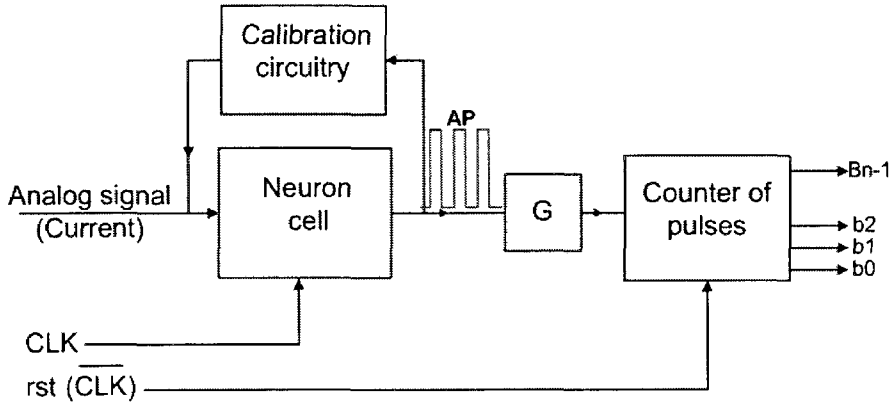


FIGURE 5.1: Block diagram of the neuromimetic ADC (Adapted from Yakoub *et al.* (2009))

output with number proportional to the input current. Figure 5.2 shows the neuron cell circuit. Initially, the membrane voltage, V_m, is zero, and the switches (SW1 and SW2) are off. As a current is applied to the input, the capacitor C starts charging linearly until V_m reaches the threshold voltage of the buffer (V_{thb}), which is equal to $VDD/2$, and the buffer output reaches the high state. This turns SW2 on, resulting in quickly discharging of capacitor C, causing V_m to drop below V_{thb}, and consequently the neuron cell output to drop down. This process is repeated several times during the sampling period, i.e., when SW1 is off. The frequency at the output of this module is calculated according to

$$f = \frac{I}{C\ V_{thb}}, \tag{5.1}$$

where I represents the input current, C denotes the membrane capacitance, and V_{thb} is the threshold voltage of the buffer.

2. *The Calibration Circuit*

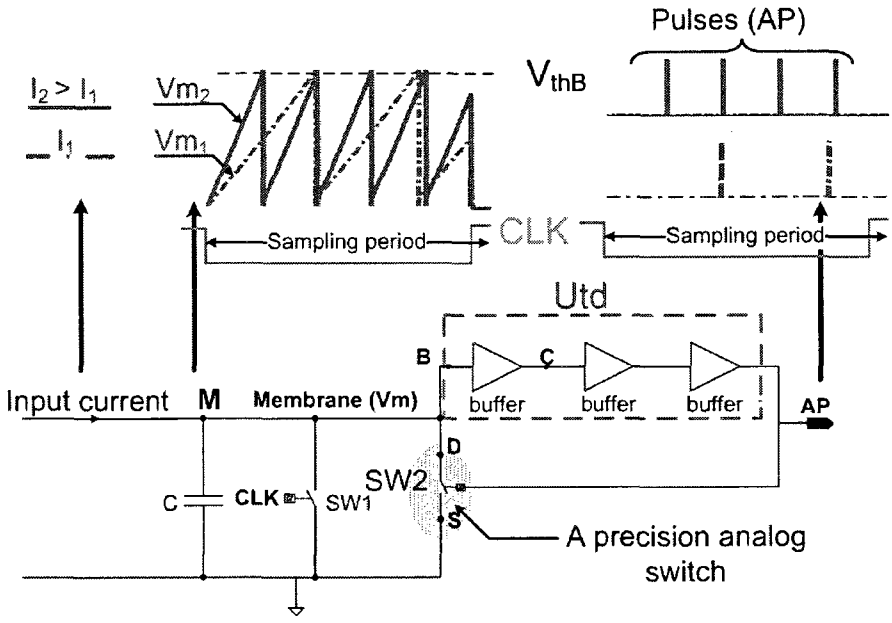


FIGURE 5.2: Neuron cell circuit, showing the waveforms at various nodes in the circuit (Adapted from Yakoub *et al.* (2009))

As reported in equation 5.1, the number of pulses at the neuron cell output is proportional to the input current. Figure 5.3 shows the calibration circuit. This is not the case in practice, which directly impacts the full scale input current (I_{FSR}) and the INL of the ADC. In order to satisfy the proportionality, a calibration circuit has been employed. This circuit works as a compensation circuit, injecting more input charge controlled by the generated pulses (APs). During each pulse, the gates of M9, M10 and M11 are high, which turns off M9, and turns on M10 and M11, resulting in M12 being turned on, acting as a current source in the presence of a pulse, and thus injecting an additional charge.

3. *The Counter*

A systolic asynchronous counter has been employed in this architecture in order to meet the low-power goal. This counter architecture consists of two blocks, each

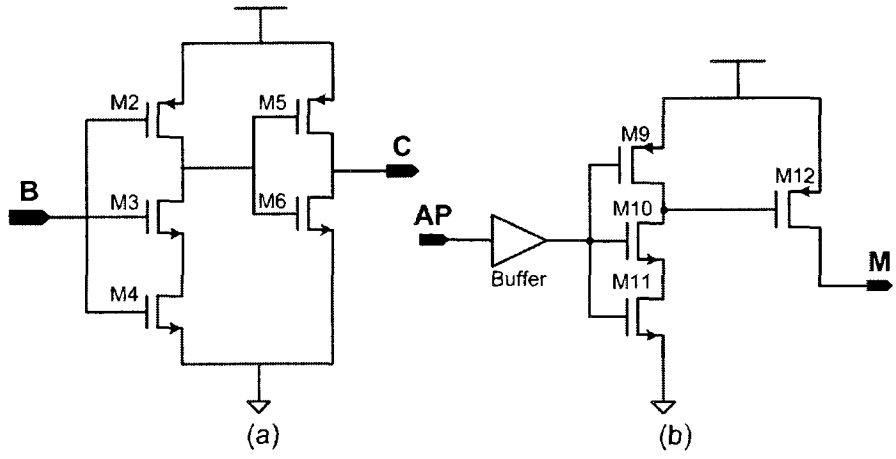


FIGURE 5.3: (a) The buffer circuit, and (b) the calibration circuit (Adapted from Yakoub *et al.* (2009))

implementing four bits (Kakarountas *et al.* (2003)). The frequency of the counter's input signal increases with the increasing input current until it reaches a maximum of 128 MHz. So this architecture is a suitable choice, since it has a frequency counting ability. After the capacitance is completely discharged by the CLK signal, i.e., at the start of a new sampling period, the counter is reset by the $\overline{CLK}$.

5.2.1 Characteristics

The digital section of this ADC was implemented using standard cells with power consumption approximated by

$$P = f_{clk}\ V_{DD}^2\ C_{ckt}\ \alpha(V_{in}), \tag{5.2}$$

where f_{clk} denotes the clock frequency, C_{ckt} represents the total capacitance of the digital circuits at the nodes of interest, and $\alpha(V_{in})$ is the switching activity factor depending on the analog input V_{in}. The ADC achieves an ultra-low energy dissipation of 5.46 pJ/cycle operating at a sampling rate of 500 kS/s and using a 1.5 V supply.

TABLE 5.1: Specifications of the NC-ADC (Yakoub *et al.* (2009))

V_{DD}	1.5 V
Capacitance C	100fF
Input range	0.1 μA - 16 μA
Sampling rate	500 kS/s
Number of bits	8
DNL	0.16 LSB*, 0.16 LSB**
INL	1.63 LSB*, 0.41 LSB**
Power consumption	486 nW

* without calibration circuit ** with calibration circuit

The total power dissipation of the ADC is 486 nW for a sampling rate of 500 kS/s.

Table 5.1 summarizes the ADC specifications. These results were obtained from post-layout simulation of the ADC.

5.3 Voltage-to-Current Converter

As explained in the previous section, the ADC we used has a current input, and the photodiode has a voltage output; so in order to digitize the data, a Voltage-to-Current converter (VCC) has to be employed to properly operate the ADC. A potential solution would be the use of an Operational Transconductance Amplifier (OTA), however several limitations with OTAs prevented their use in our project. The first one is that for low-voltage applications there is a loss of linearity in the output (Gray *et al.* (2001)). Another limitation is the offset at the differential input which would make it difficult to control the output current in the needed range (I_{FSR} of the used ADC is 16 μA). The last one is that with OTAs it is difficult to match impedance with the input of the load circuit, and resistive load will kill the gain of OTAs (Baker (2008)).

We implemented a VCC having a linear output, with a current range compatible with

the I_{FSR} of the ADC. It is an all-MOS resistorless circuit (Fotouhi (2001)).

This VCC produces an output current that is the sum of the currents in two transistors operating in the linear and saturation regions. The individual currents in the two transistors are nonlinear, however their combined currents are designed to be linear. To prove this it is best to start with the equations describing the currents in a MOS transistor.

The drain current of a MOSFET operating in the linear (triode) region is given by

$$I_D = \beta[(V_{gs} - V_t)V_{ds} - \frac{1}{2}V_{ds}^2], \tag{5.3}$$

where $\beta = \mu C_{OX} W/L$, μ is the carrier mobility, C_{OX} is the gate capacitance per square centimeter, W is the channel width, L is the channel length, V_{gs}, V_{ds}, and V_t are the gate-to-source, drain-to-source, and threshold voltage, respectively.

The drain current of a MOSFET operating in the saturation region, ignoring the channel modulation effect, is given by

$$I_D = \frac{1}{2}\beta(V_{gs} - V_t)^2. \tag{5.4}$$

Adding the currents given by equations (5.3) and (5.4) we get

$$I_{out} = \beta_1[(V_{gs1} - V_{t1})V_{ds} - \frac{1}{2}V_{ds}^2] + \frac{1}{2}\beta_2(V_{gs2} - V_{t2})^2. \tag{5.5}$$

Assuming that V_{ds} is equal to the input voltage, and $V_{gs2} - V_{t2} = V_{ds}$, and letting $\beta_2 = 2\beta_1$, equation (5.5) reduces to

$$I_{out} = \beta_1(V_{gs1} - V_{t1})V_{in}. \tag{5.6}$$

By setting $V_{gs1} - V_{t1}$ to be a fixed voltage, we get a linear relation between I_{out} and V_{in}.

The condition of $V_{gs2} - V_{t2} = V_{ds}$ is obtained by shifting V_{ds} by V_{t2} and forcing it across V_{gs2}.

The schematic diagram of the used VCC is detailed in figure 5.4. We used at the output of this VCC a wide swing current mirror instead of a simple current in order to adapt the impedances between the NC-ADC and the VCC.

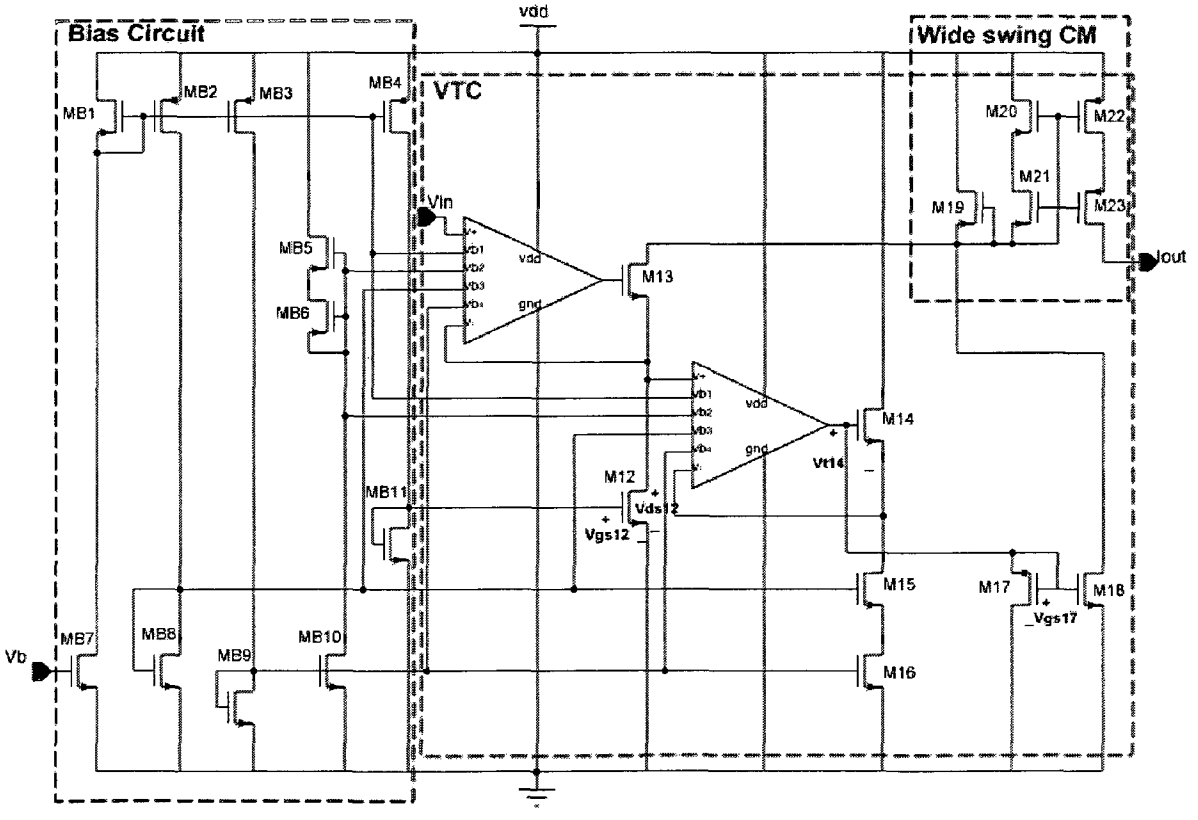


FIGURE 5.4: Schematic diagram of the all-MOS voltage-to-current converter

Transistor M12 is biased in its linear region at a fixed voltage by MB11, and its drain

current I_{12} is given by equation (5.3). Next, V_{ds12} is buffered and shifted by V_{t14}, and the result is forced across transistor M17. The current in M17 is given by equation (5.4). M18 multiplies the current in M17 by a coefficient α ($\alpha = (W/L)_{18}/(W/L)_{17}$). So, by proper sizing of M12 and M18, I_{out} will be linear as given by equation (5.6).

5.4 Post-Layout Simulation Results

The VCC has been implemented in 0.18 μm CMOS process. In this section we will provide the post-layout simulation results for the whole circuit including the VCC and the NC-ADC.

5.4.1 The Voltage-to-Current Converter

The layout implementation of the VCC is shown in figure 5.5. We simulated the extracted layout with a voltage ramp input going from 0 V to 660 mV. The simulation result is shown in figures 5.6 and 5.7.

Figure 5.6 shows the simulation result for the currents I_{12} (drain current of M12), I_{18} (drain current of M18) and I_{out}. I_{12} changes quadratically until it saturates at $V_{in} =$ 660 mV. I_{18} starts linearily and then saturates as M18 enters its saturation region with increasing V_{in}. the output I_{out} which is the sum of I_{12} and I_{18} increases linearily and saturates at $V_{in} = 660\ mV$. From this graph we could observe the linear relation between V_{in} and I_{out}, from 0 V to 660 mV. In this region, the relation between the output current and the input voltage is given by: $I_{out} = 2.65 \times 10^{-5}\ V_{in}$.

Figure 5.7 illustrates the direct proportionality between I_{out} and V_{in}. It can be noticed that the VCC saturates at an input voltage of 660 mV, which is high enough for our application, since the photodiode output is in the range of 0 V to 650 mV. The current output range of this module is between 285 nA and 15.3 μA, which is also

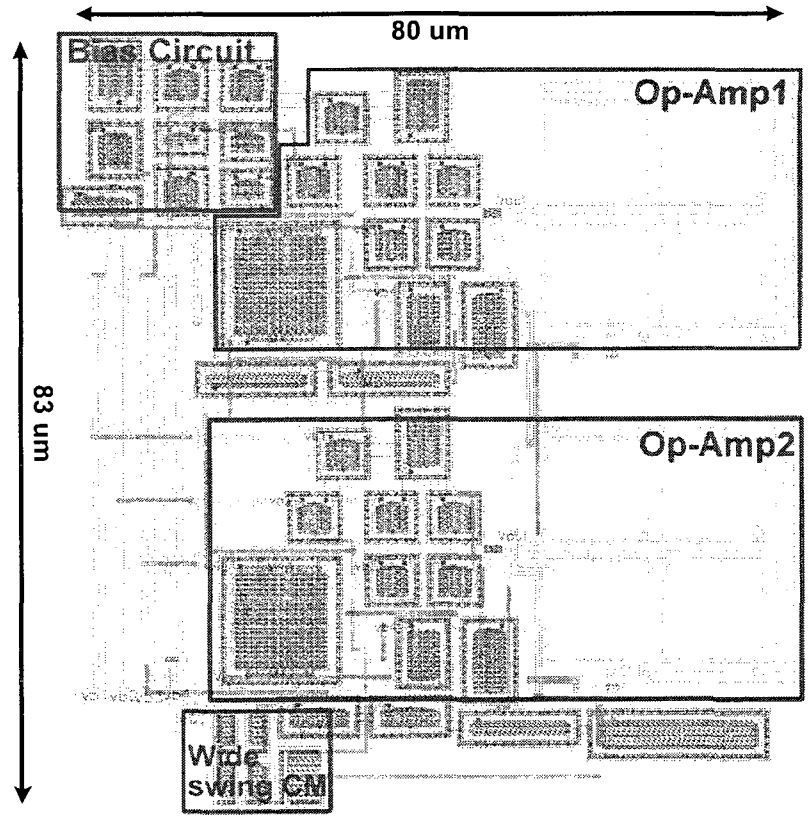


FIGURE 5.5: Layout of the VCC

suitable for our application, since the full scale range input current (I_{FSR}) of the ADC, as mentionned in Table 5.1, is 16 μA. The power consumed by this module is 80 μW, for a power supply of 1.5 V.

5.4.2 NC-ADC

The layout of the NC-ADC was implemented in a standard 0.18 μm CMOS process. The core layout of this ADC occupies an area of 0.05 mm^2.

Figure 5.8 illustrates the layout of the NC-ADC. Once the VCC was tested, we coupled it with the ADC to verify its functionnality. The testbench consisted of the VCC, the NC-ADC and an 8-bit ideal Digital-to-Analog Converter (DAC) coded in `veriloga`.

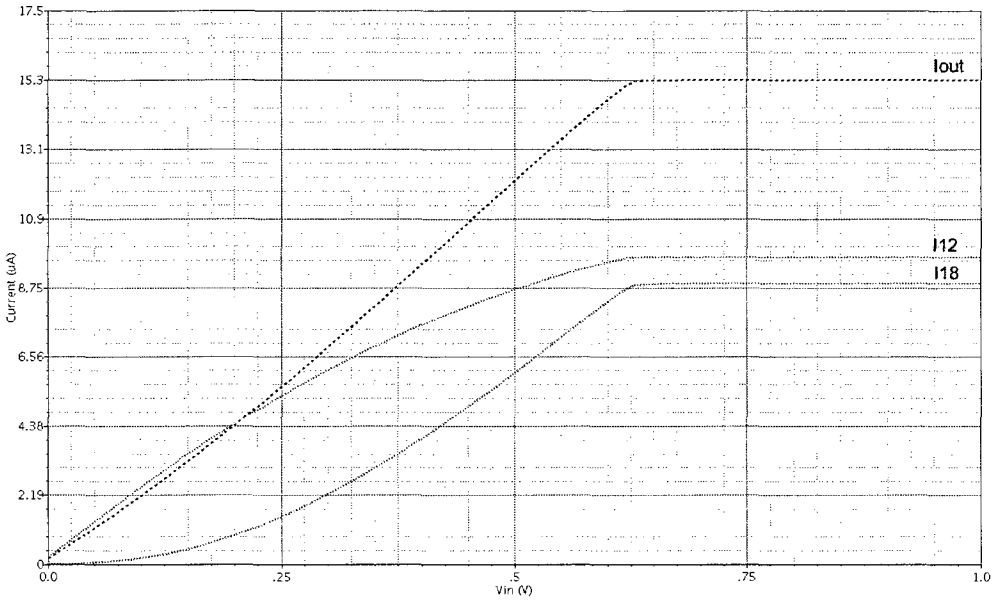


FIGURE 5.6: The VCC output current versus the input voltage

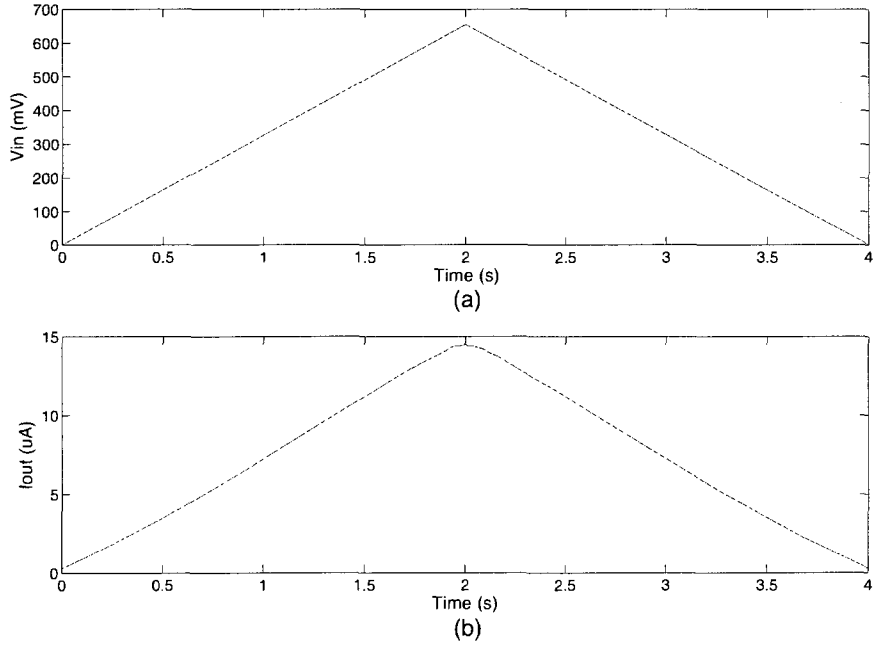


FIGURE 5.7: Post-layout simulation results of the VCC: (a) input voltage, (b) output current

The DAC was used to reconstruct the output of the NC-ADC in order to compare it with the input signal, and verify the integrity of the circuit.

Figure 5.9 shows the voltage input of the whole system, going from 0 to 800 mV, and the current input of the ADC, which is the output of the VCC, going from 285 nA and saturating at 15.3 μA.

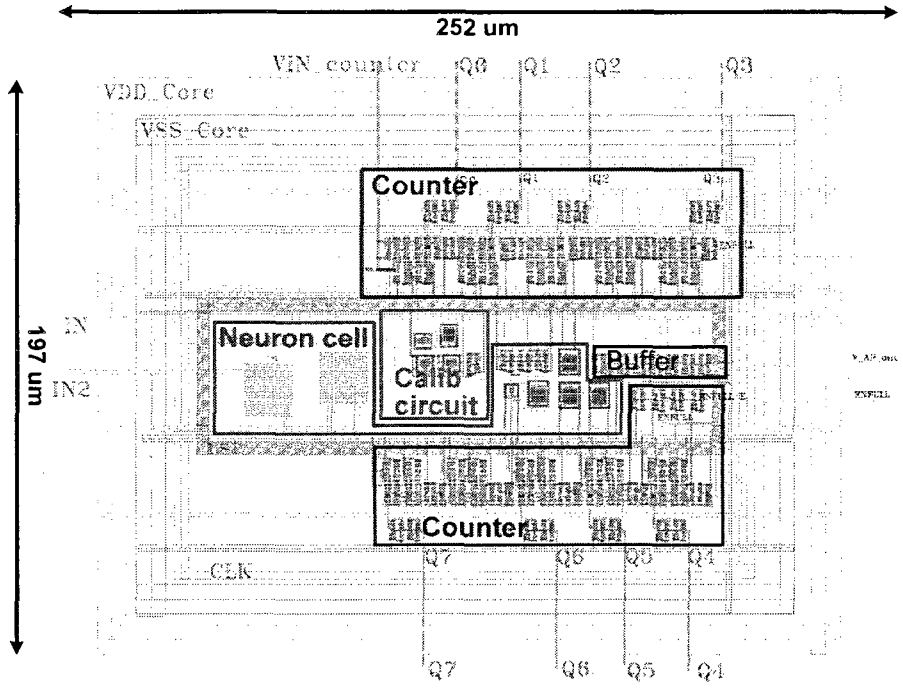


FIGURE 5.8: Layout of the NC-ADC

Figure 5.10 illustrates the voltage output of the DAC, representing the digital output of the NC-ADC. We could notice the curve saturates at 1.45 V, instead of the full-scale (1.5 V). This is due to the fact that the current input not reaching the I_{FSR} of the ADC which is 16 μA.

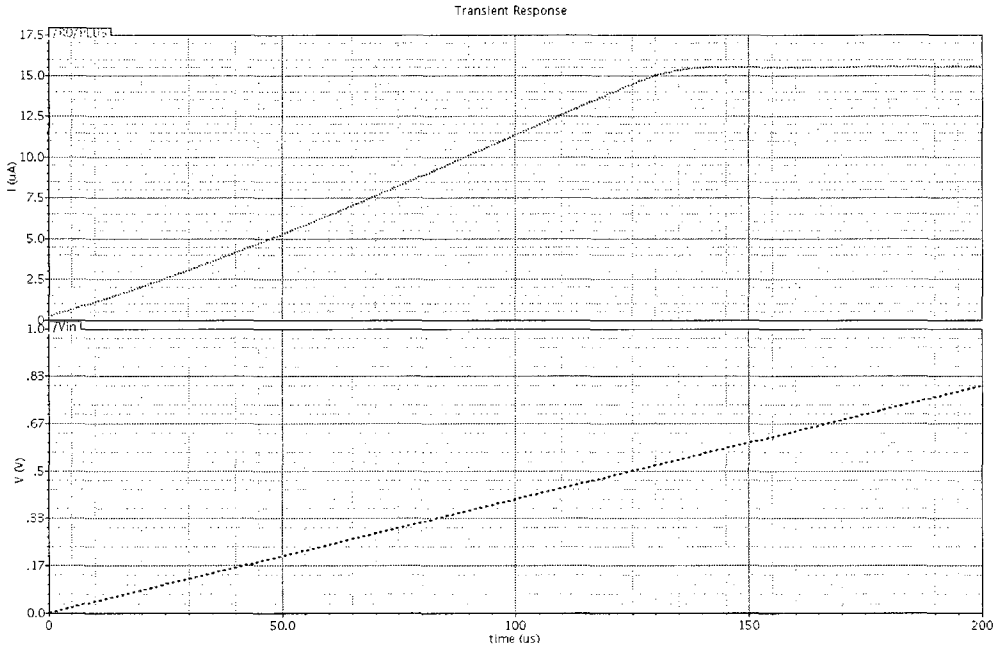


FIGURE 5.9: Voltage input of the system, and current input of the ADC

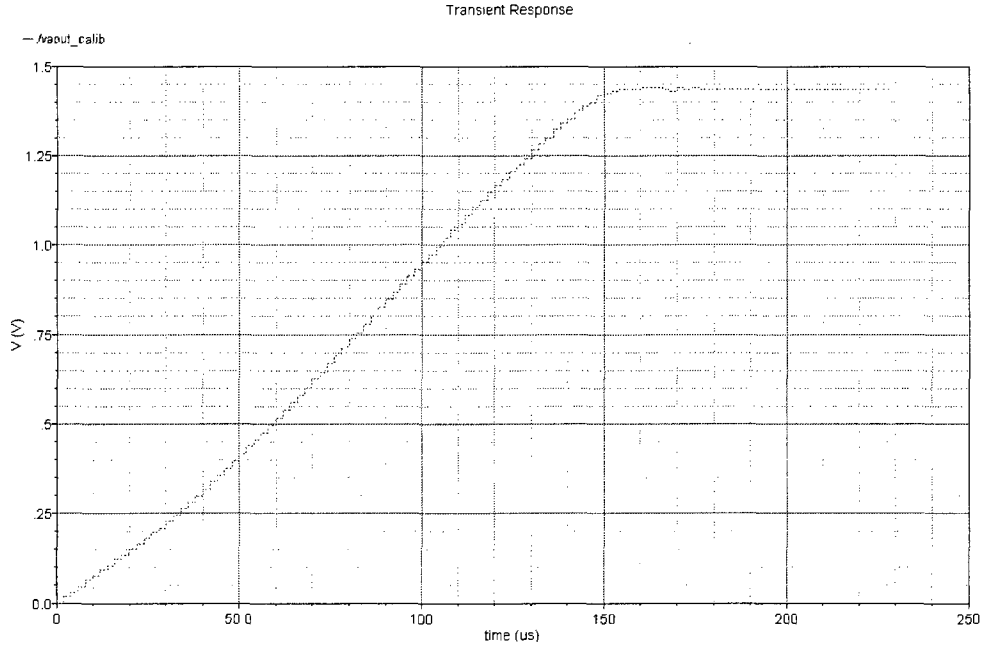


FIGURE 5.10: Voltage output of the DAC representing the digital output of the NC-ADC

5.4.3 Controller

The serial-to-parallel register, initially included in the design of the control module for the discrete ADC, was removed, since the custom NC-ADC has an 8-bit parallel output. To reduce the simulation time also, the counters at the output of the control module were removed, so the output is in the form of either a logic '1' (ON) or a logic '0' (OFF).

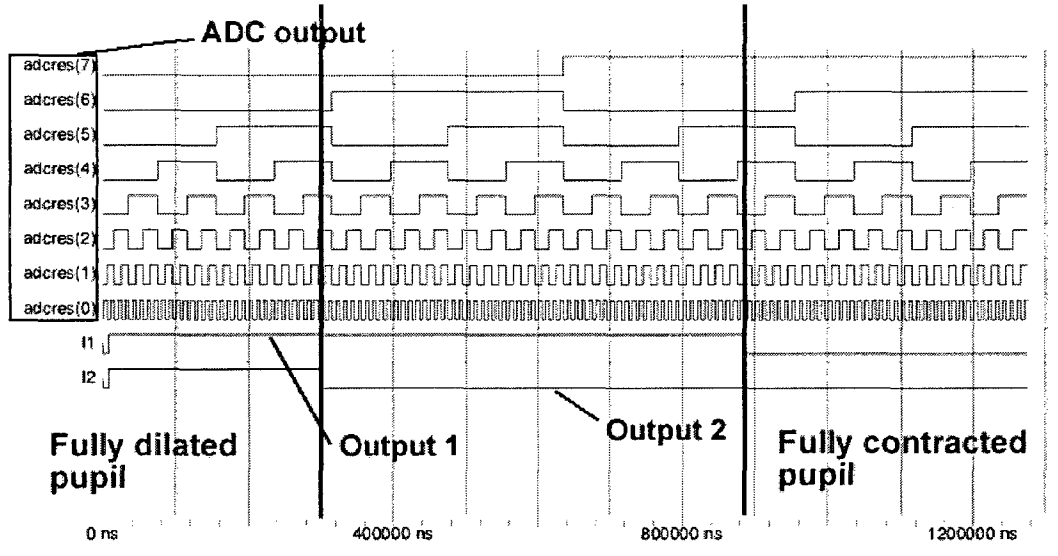


FIGURE 5.11: Simulation results of the controller with the parallel-output ADC

Functional simulation results of the ADC and controller are illustrated in figure 5.11. We can see how the controller outputs both start 'ON' giving a fully dilated pupil, then with the increasing ADC input, i.e., increasing luminosity, first output L2 goes 'OFF', then output L1 goes 'OFF', giving a fully constricted pupil.

5.5 Recapitulation

In this chapter we presented a fully integrated version of the system presented in chapter 4, by implementing an ADC to make the whole system more compact. We

employed an ADC developped by the Polystim Neurotechnologies Laboratory, and we developed a voltage-to-current converter in order to be able to use the ADC with our system.

Simulations were carried on, and good results were obtained, proving what was expected.

These circuits could be used later in the fabrication of a new more compact chip and would be integrated to the proposed system.

CONCLUSION

Nowadays ocular prosthetics are being more and more improved in order to give a more realistic look to patients with an eviscerated or enucleated eye. However, cosmetics are compromised due to the static pupils of present-day ocular prosthesis, which do not respond to light intensity variations.

This master thesis deals with a fully integrated rehabilitation system. The objective of this work is to overcome the problem of post-prosthetic anisocoria. This is done by replacing the static pupils of present-day ocular implants with a prosthetic dynamic pupil. By doing so, the problem of post-prosthesis anisocoria could be solved, and the implant would resemble the natural eye.

This system simulating the human iris, has a circular form with a diameter of 12 mm, and a thickness of 6 mm. This system is composed of a controller, a display and a photosensitive cell. The controller is implemented in 0.18 μm CMOS technology with a size of 1.05 mm x 1.25 mm; the display is constituted of 114 mini-LEDs each having a size of 1.0 mm x 0.5 mm forming the circular display; and the photodetector is a commercially available photodiode (TDK, Garden City, NY) having a size of 1.5 mm x 2 mm and a spectral sensitivity area between 350 and 750 nm.

The role of the controller is to take light information from the photocell, transform it to light intensity (lux), compare it with stored values and finally to control the display suitably so as to give the appearance of a contracted pupil in strong lights and dilated pupil in dim lights.

Finally, we proposed to integrate the ADC on-chip, in order to reduce the occupied space. So, we employed an ADC developed by the Polystim team, and we developed a voltage-to-current converter in order to be able to use the ADC with the needed photodiode.

As for the recommendations for future work, we suggest:

- The use of LCD technology to develop the prosthetic pupil instead of LEDs. This way energy consumption could be reduced, and an optimum cosmetic result could be obtained. We propose to employ a liquid crystal module in a concentric ring fashion, and each ring would be controlled individually.

- The fabrication of the integrated circuit containing the ADC and VCC proposed in chapter 5, so the system would become more compact, and also reduce energy consumption.

- The integration of natural eye movement to the ocular implant, to allow for the prosthetic eye to move in synchrony with the natural eye, giving patients a much more realistic prosthesis. It would also be interesting to investigate the possibility of incorporating artificial vision to this work, since in the majority of times, the optic nerve of patients who have lost an eye is intact.

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APPENDIX I

DIGITAL DESIGN FLOW

The digital design flow on which our design was based:

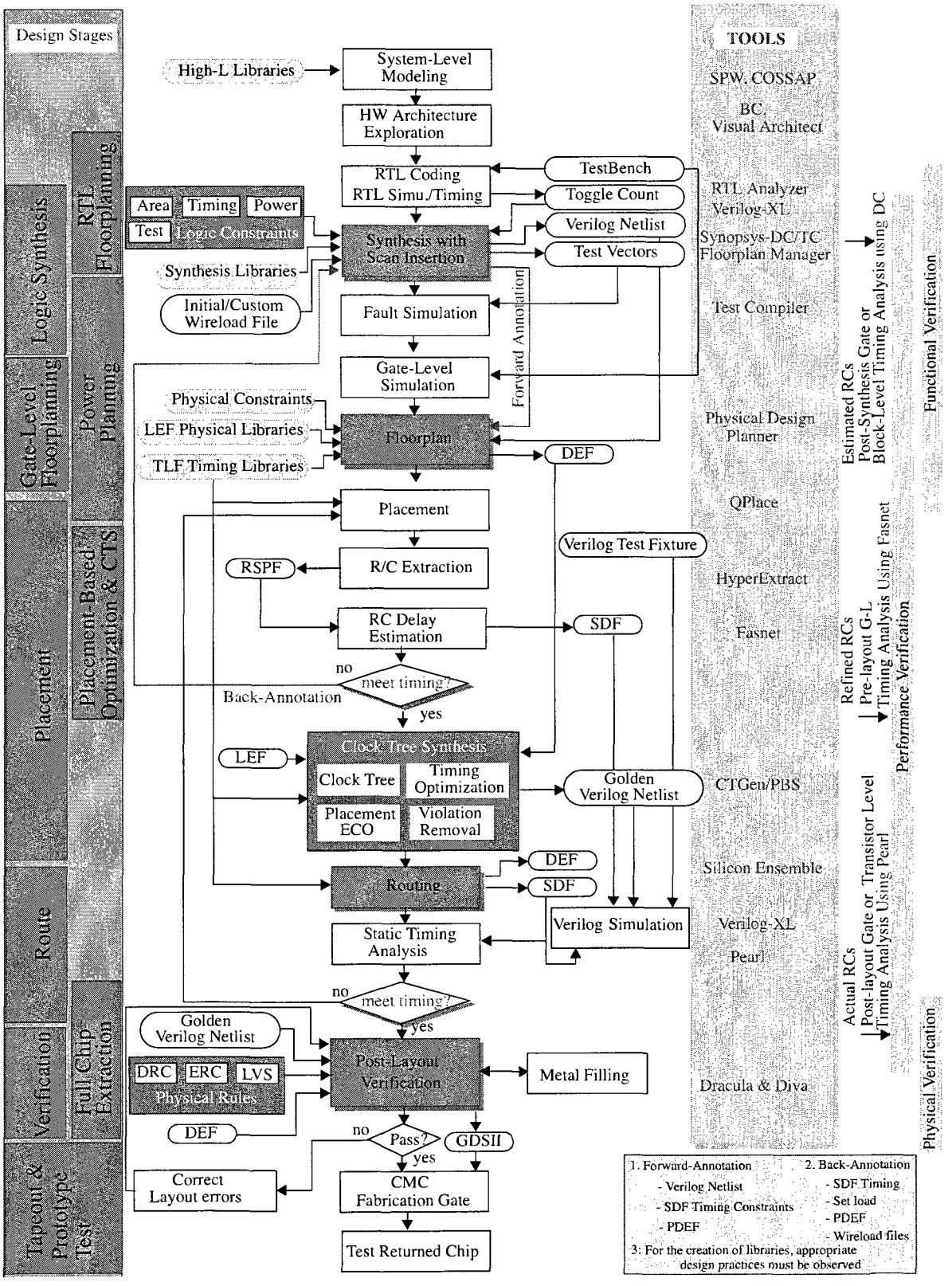

FIGURE I.1: The digital design flow provided by CMC (Used with permission)